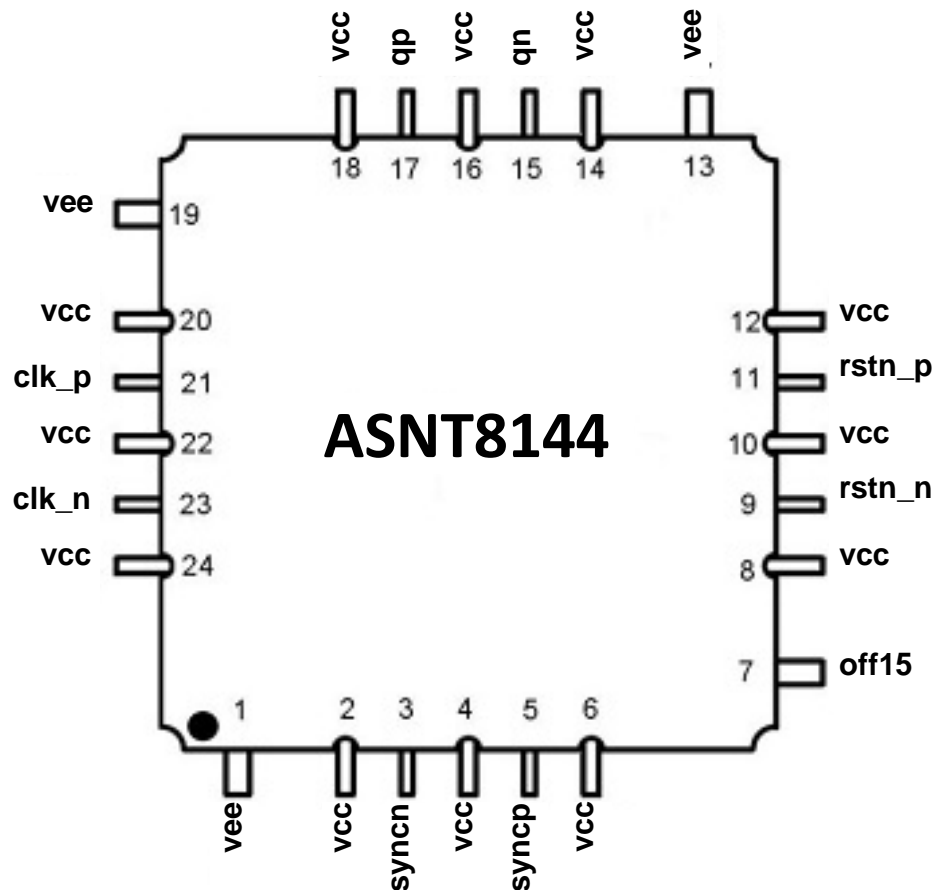


ASNT8144-KMC

Generator of DC-to-23Gbps PRBS with Selectable Polynomials and a Synchronization Signal

- Full-length ($2^{15}-1$) or (2^7-1) pseudo-random binary sequence (PRBS) generator
- Selectable power of the Polynomial
- DC to 23Gbps output data rate
- Additional output for a synchronization signal
- Asynchronous reset signal for elimination of the “all zeros” initial state
- Fully differential CML input interface
- Fully differential CML output interface with 400mV single-ended swing
- Single +3.3V or -3.3V power supply
- Power consumption: 850mW
- Custom CQFP 24-pin package



DESCRIPTION

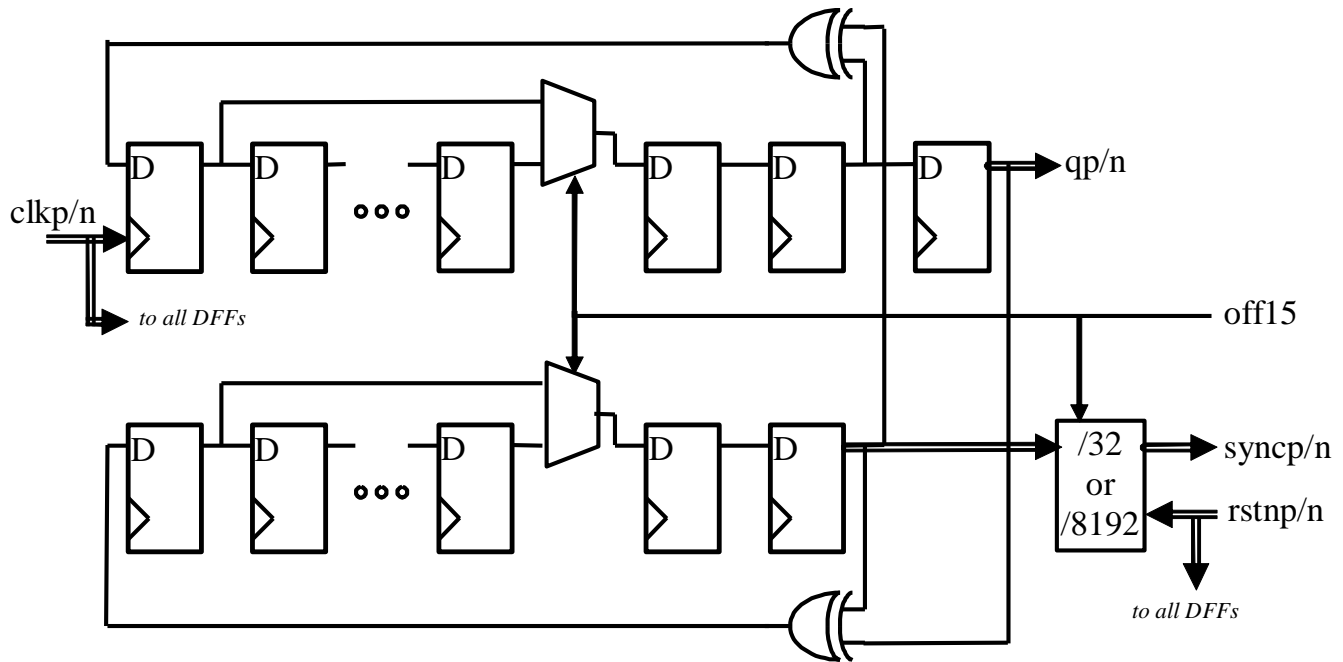


Fig. 1. Functional Block Diagram

The part shown in Fig. 1 provides a selectable full 32767-bit or 127-bit long pseudo-random binary sequence (PRBS) signal according to either a $(x^{15} + x^{14} + 1)$, or a $(x^7 + x^6 + 1)$ polynomial respectively, where x^D represents a delay of D clock cycles. This is implemented as a linear feedback shift register (LSFR) in which the outputs of either the fifteenth and fourteenth, or seventh and sixth flip-flops are combined together by an XOR function, and provided as an input to the first flip-flop of the register. The polynomial is selected through the external control signal **off15**.

The LSFR-based PRBS generator produces all possible binary states, excluding the “all zeros” state that is illegal for the XOR-based configuration. To eliminate this state that locks the LSFR and prevents PRBS generation, an asynchronous external active-low preset signal **rstnp/rstnn** is implemented in the circuit. When the preset is asserted, LSFR is set to the “all ones” state that is enough for activation of the PRBS generation. When the preset is released, the chip delivers one consecutive bit of the PRBS signal to output pins **qp/qn** per each rising edge of clock **clkp/clkn**, starting from the above mentioned state.

A synchronization signal with one pulse per PRBS period is generated by the sequence division by either 32 or 8192, and is delivered to pins **syncp/syncn**. A simulated example of the synchronization signal in case of division by 32 is shown in Fig. 2.

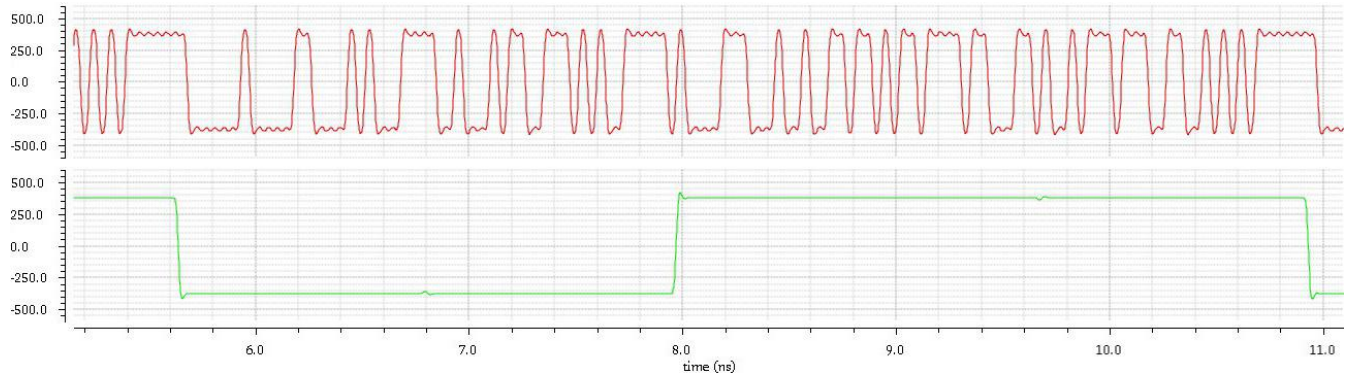


Fig. 2. PRBS7 output and Sync output Diagram (Simulation)

The simulated eyes for PRBS signals are shown in Fig. 3.

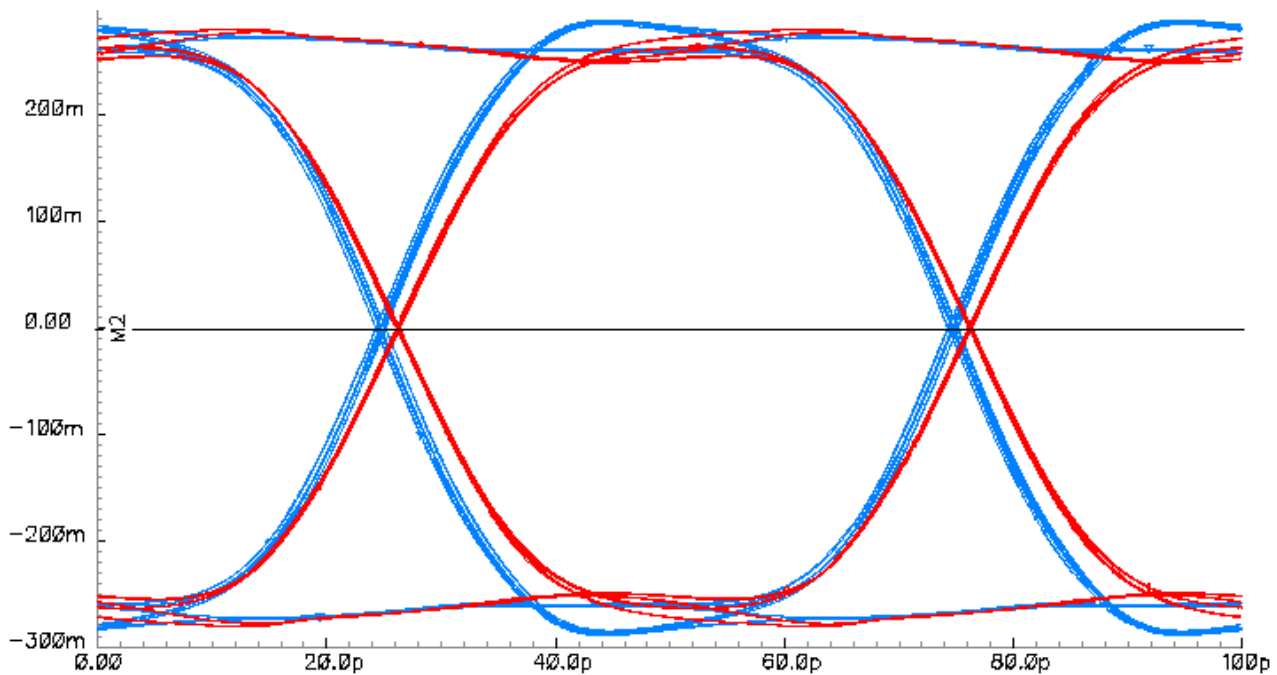


Fig. 3. 20Gbps PRBS Output Eye Diagram (Simulation, Slow Corner, 125°C)

All I/O stages are back terminated to v_{cc} with on-chip 50Ω resistors and may be used in either DC or AC coupling modes (see also POWER SUPPLY CONFIGURATION). In the first mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the second mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

POWER SUPPLY CONFIGURATION

The part can operate with either a negative supply ($v_{cc} = 0.0V = \text{ground}$ and $v_{ee} = -3.3V$), or a positive supply ($v_{cc} = +3.3V$ and $v_{ee} = 0.0V = \text{ground}$). In case of a positive supply, all I/Os need AC termination when connected to any devices with 50Ω termination to ground. Different PCB layouts will be needed for each different power supply combination.



All the characteristics detailed below assume $V_{CC} = 0.0V$ and $V_{EE} = -3.3V$.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed V_{CC}).

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (V_{EE})		-3.6	V
Power Consumption		0.86	W
RF Input Voltage Swing (SE)		1.0	V
Case Temperature		+90	$^{\circ}C$
Storage Temperature	-40	+100	$^{\circ}C$
Operational Humidity	10	98	%
Storage Humidity	10	98	%

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	No.	Type	
High-Speed I/Os			
rstn_p	11	CML input	Differential high-speed asynchronous reset (active low) inputs with internal SE 50 Ω termination to V_{CC}
rstn_n	9		
clk_p	21	CML input	Differential clock input signals with internal 50 Ω termination to V_{CC}
clk_n	23		
qp	17	CML output	Differential data outputs. Require external SE 50 Ω termination to V_{CC}
qn	15		
syncp	5	CML output	Differential synchro signal outputs. Require external SE 50 Ω termination to V_{CC}
syncn	3		
Control Signal			
off15	7	CMOS input	3.3V CMOS input with internal 1M Ω termination to V_{CC}
Supply and Termination Voltages			
Name	Description		Pin Number
vcc	Positive power supply (+3.3V or 0)		2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24
vee	Negative power supply (0V or -3.3V)		1, 13, 19



ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.1	-3.3	-3.5	V	±6%
vcc		0.0		V	External ground
I _{vee}	240		275	mA	
Power consumption		850		mW	
Junction temperature	-40	25	125	°C	
HS Input Clock (clkp/clkn)					
Frequency	DC		23	GHz	
Swing	0.05		0.8	V	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	V	Must match for both inputs
HS Output Data (qp/qn)					
Swing (SE)	280	440		mV	
CM Voltage Level	vcc-0.8		vcc	V	
Output Jitter		2.5		ps	Peak-to-peak
LS Output Data (syncp/syncn)					
Swing (SE)	280	440		mV	
CM Voltage Level	vcc-0.8		vcc	V	
Reset Signal (rstnp/rstnn)					
Frequency	DC		15	GHz	
Rise time			20	%	of the clock period
Recovery time	36			ps	
Swing	0.05		0.8	V	Differential p-p
CM Voltage Level	vcc-0.8		vcc	V	
PRBS Select Signal (off15)					
Input low level	vee		vee+0.4	V	Do not apply voltages below vee!

PACKAGE INFORMATION

The chip die is housed in a custom 24-pin CQFP package shown in Fig. 4. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the vcc plain, which is ground for a negative supply, or power for a positive supply.

The part's identification label is ASNT8144-KMC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with Commission Delegated Directive (EU) 2015/863 of 4 June 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances (Text with EEA relevance) on the restriction of the use of certain hazardous



substances in electrical and electronics equipment (RoHS Directive) in accordance with the definitions set forth in the directives for all ten substances.

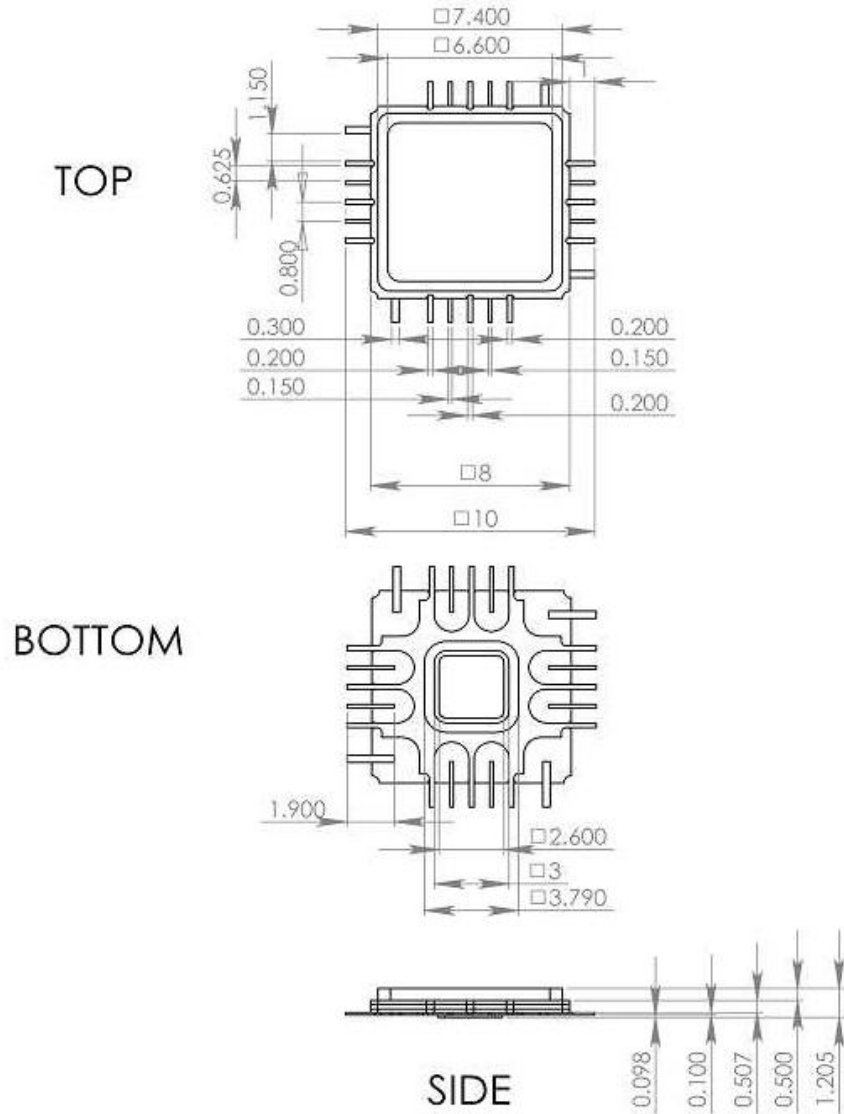


Fig. 4. CQFP 24-Pin Package Drawing (All Dimensions in mm)

REVISION HISTORY

Revision	Date	Changes
1.0.2	06-2021	First Release
0.1.1	04-2021	Added Fig. 2
0.0.1	11-2020	Preliminary release