



# User Guide

## EVB-ATEK252N3-02

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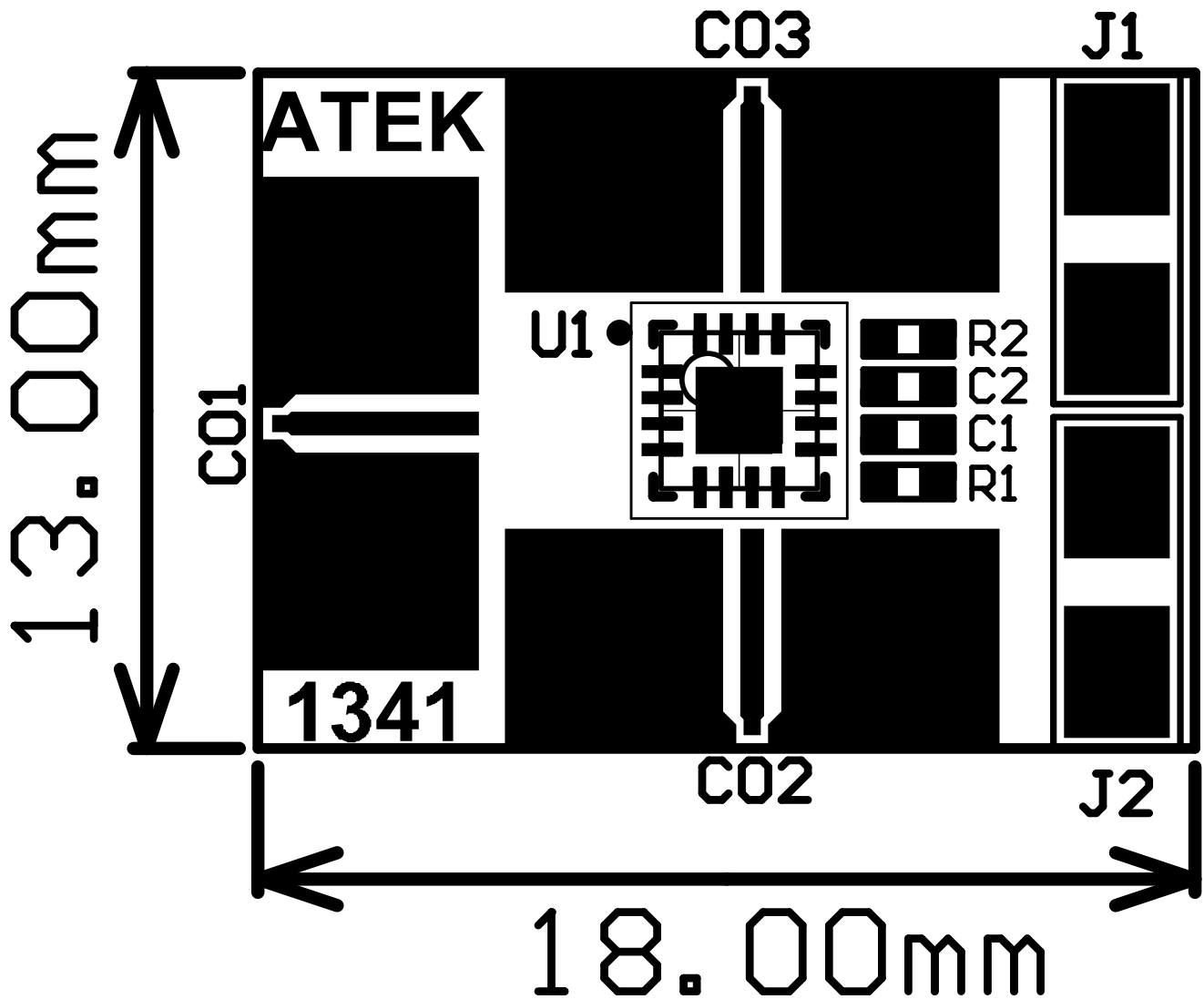
**Revisions**

Revision No	Revision Date	Revision Reason	Section / Page No
1.0	08.07.2021	Initial Version	
1.1	08.01.2022	Format and Content Fixed	
1.2	16.04.2022	Format and Content Fixed	

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1 GENERAL INFORMATION



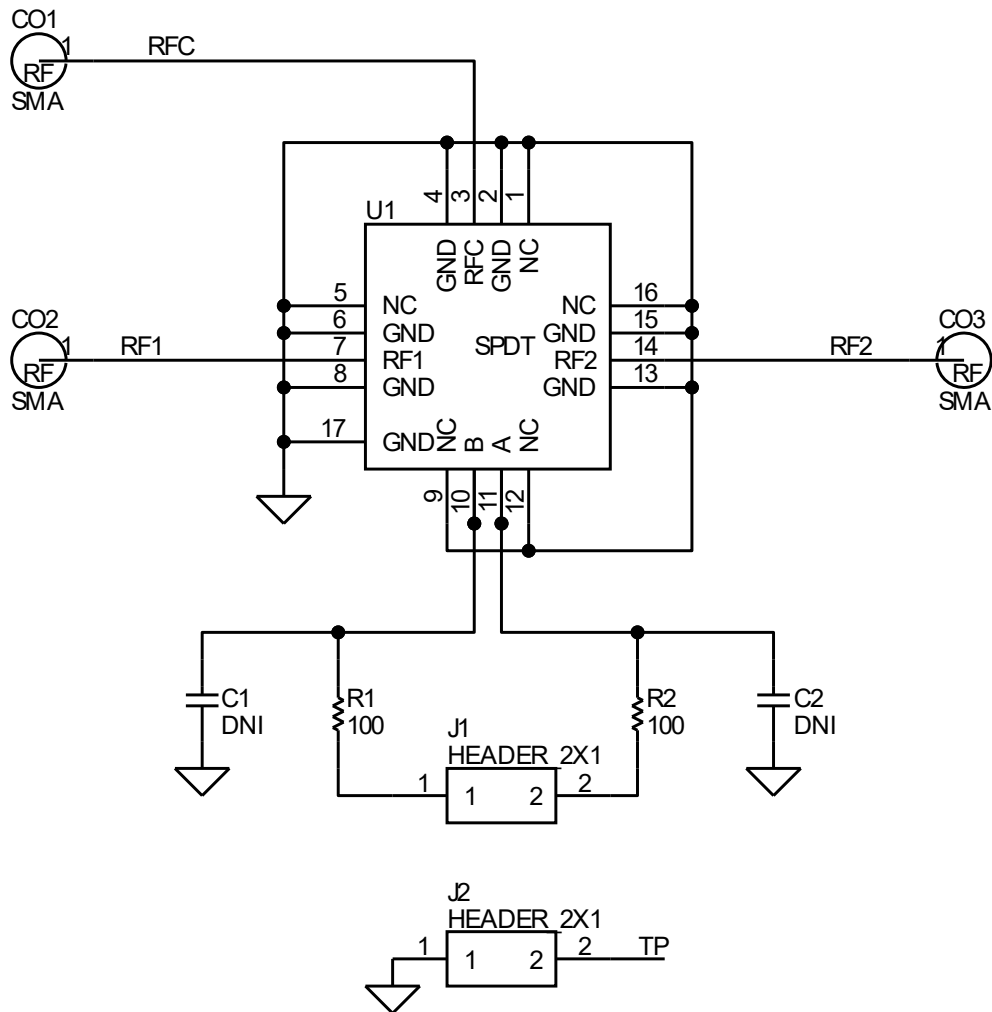
PIN Name	Definition	Comment
<b>CO1</b>	RF IN	K Connector
<b>CO2, CO3</b>	RF OUT	K Connector
<b>J1 Up</b>	CTRL A	2.54mm Header
<b>J1 Down</b>	CTRL B	2.54mm Header
<b>J2 Up</b>	N/A	2.54mm Header
<b>J2 Down</b>	GND	2.54mm Header

Notes:

1. VDD Voltage is detailed in Datasheet.
2. Control Voltage is detailed in Datasheet.
3. The definition of up, down, right, and left is valid for this view of PCB.

2 DESIGN INFORMATION

2.1 SCHEMATIC



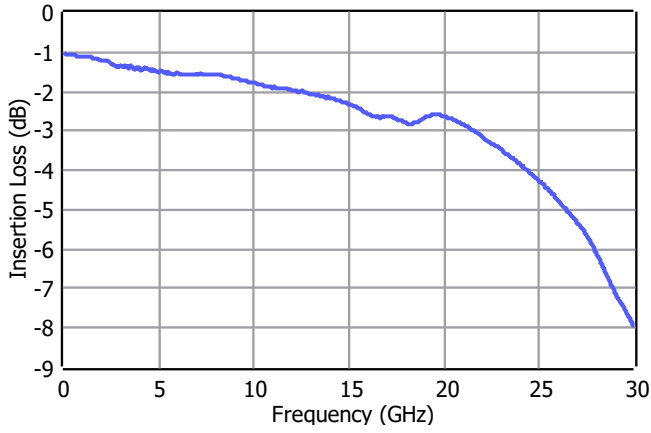
2.2 BOM

Designator	Footprint	Qty	Comment	PN
<b>C1, C2</b>	0402	2	DNP	
<b>CO1, CO2, CO3</b>	K Connector	3	K Connector	ATEK9292
<b>J1, J2</b>	2x1 Header	2	2x1 Header	
<b>R1, R2</b>	0402	2	OR	
<b>U1</b>	ATEKQ3316	1	SPDT	ATEK252N3

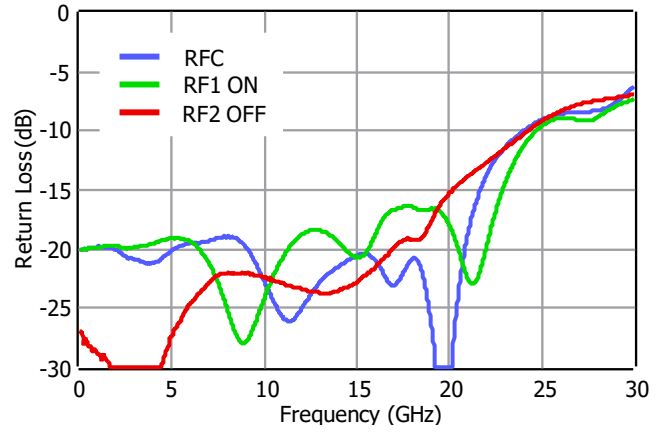
3 TYPICAL PERFORMANCE PLOTS

Conditions unless otherwise specified:  $V_{CTRL} = 0/-5$  V,  $T = 25$  C, CW. For details, please refer to the datasheet.

Insertion Loss



Return Loss



Isolation from RFC to RF2

