


| | | | |
|--|------------|------------------|------------|
| MDT0280A1IH-MULTI | 240 x 320 | Multi Interface | TFT Module |
| (MCT028D0W240320PMLIPS) Specification | | | |
| Version: 1 | | Date: 21/01/2015 | |
| Revision | | | |
| 1 | 20/01/2015 | First issue | |

| Display Features | |  |
|-----------------------|------------------------|---|
| Display Size | 2.8" | |
| Resolution | 240 x 320 | |
| Orientation | Portrait | |
| Appearance | RGB | |
| Logic Voltage | 3.3V | |
| Interface | Multi | |
| Brightness | 500 cd/m ² | |
| Touchscreen | --- | |
| Module Size | 50.50 x 69.70 x 2.60mm | |
| Operating Temperature | -20°C ~ +70°C | |
| Pinout | 50 way FFC | |
| Pitch | 0.5mm | Weight / Display |
| | | --- |
| | | --- |

* - For full design functionality, please use this specification in conjunction with the ST7789V specification.(Provided Separately)

| Display Accessories | |
|---------------------|---|
| Part Number | Description |
| MPBV5 Kit | Interconnect board that converts a 50-way FFC to 50 crimp-wire connector. |
| MCIB-12 | Uno32 Break-out Board with SD Card and LED Backlight Driver. The MCIB-12 Board can be used for any display with a 4 bit, 8 bit, I2C or SPI interface. |
| | |

| Optional Variants | |
|-------------------|---------|
| Appearances | Voltage |
| | |



General Description

* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This model is composed of a Transmissive type TFT LCD Panel, driver circuit, back-light unit. The resolution of a 2.8" TFT-LCD contains 240x320 pixels, and can display up to 65K/262K colors.

* Features

-Low Input Voltage: 3.3V(TYP)

-Display Colors of TFT LCD: 65K/262K colors

-RGB Interface: 8/9/16/18BIT 8080 MCU interface;3/4-wire serial interface;16/18BIT RGB

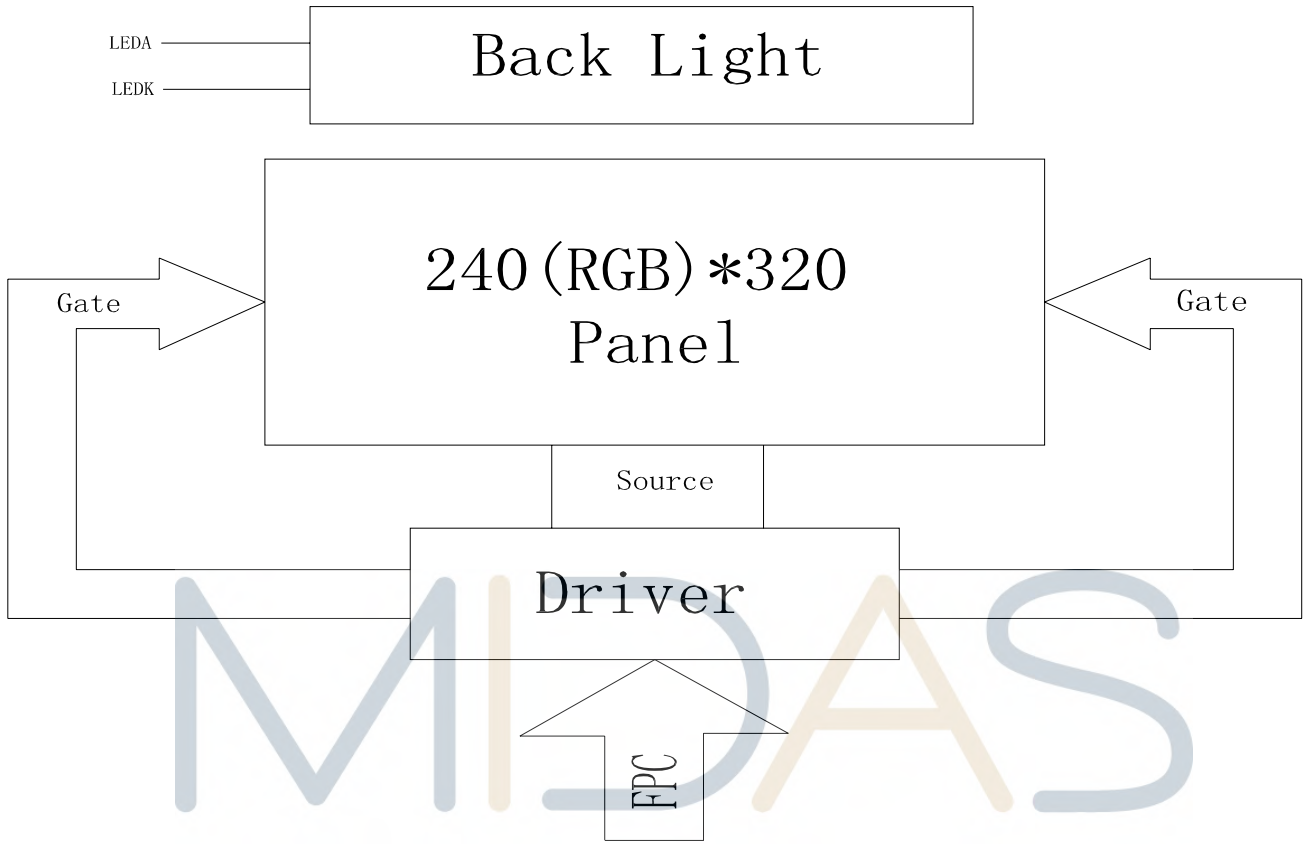
| General Information Items | Specification | Unit | Note |
|---------------------------|------------------------------|-----------|------|
| | Main Panel | | |
| Display area(AA) | 43.20(H)*57.60 (V) (2.8inch) | mm - | |
| Driver element | TFT active matrix | - | - |
| Display colors | 65K/262k | colors | - |
| Number of pixels | 240(RGB)*320 | dots | - |
| Pixel arrangement | RGB vertical stripe | - | - |
| Pixel pitch | 0.153(H)*0.153(V) | mm | - |
| Viewing angle | ALL | o'clock - | |
| Controller IC | ST7789V | - | - |
| Display mode | Transmissive/ Normally black | - | - |
| Operating temperature | -20~+70 | °C | - |
| Storage temperature | -30~+80 | °C | - |

* Mechanical Information

| Item | | Min. | Typ. | Max. | Unit | Note |
|-------------|---------------|------|-------|------|------|------|
| Module size | Horizontal(H) | | 50.50 | | mm | - |
| | Vertical(V) | | 69.70 | | mm | - |
| | Depth(D) | | 2.60 | | mm | - |
| Weight | | TBD | | | g | - |



Block Diagram

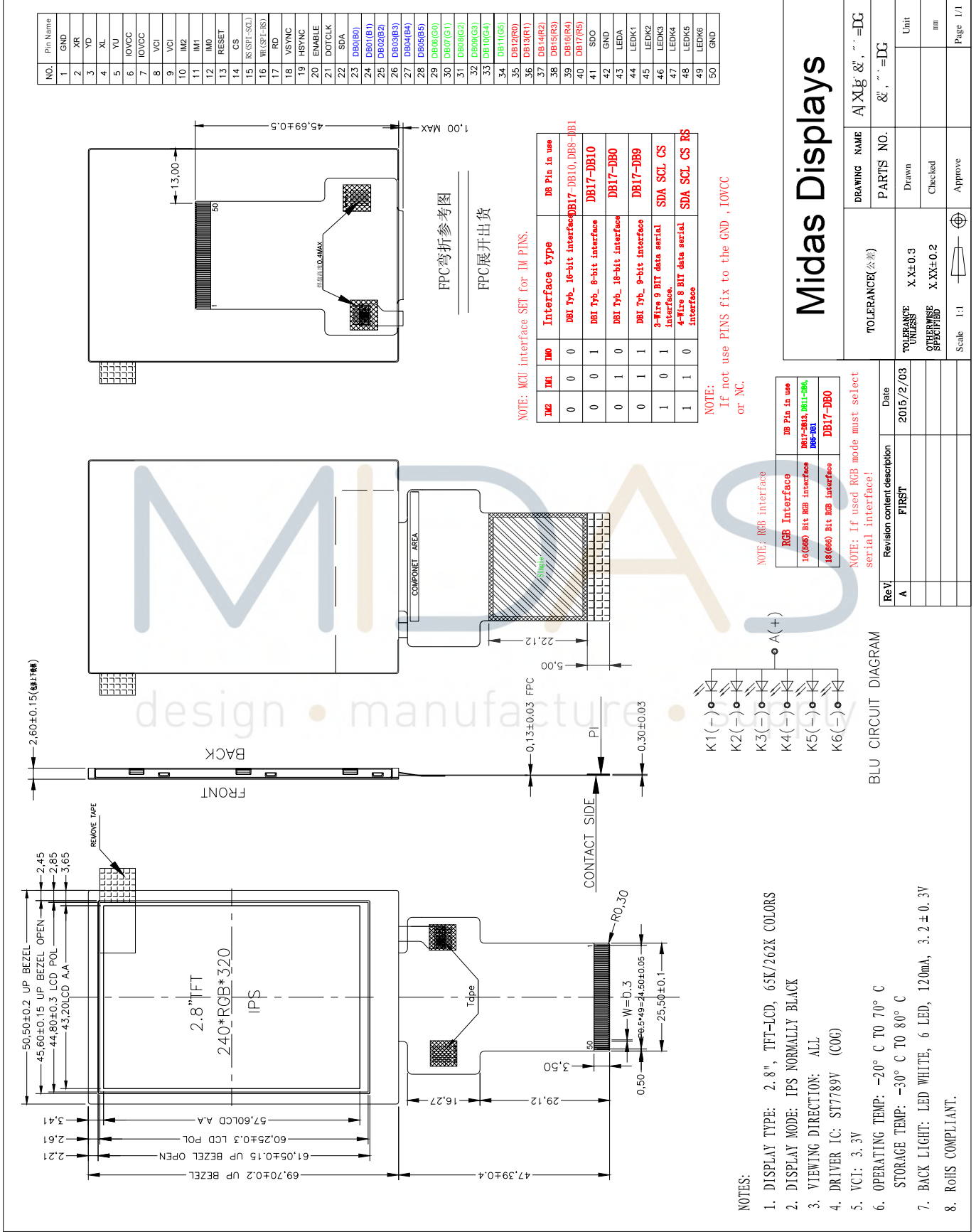


MILIDAS

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Outline dimension



Input terminal Pin Assignment

| NO. | SYMBOL | DISCRIPTION | I/O |
|-----|-------------|---|-----|
| 1 | GND | Ground. | P |
| 2 | XR(NC) | Touch panel Right Glass Terminal | A/D |
| 3 | YD(NC) | Touch panel Bottom Film Terminal | A/D |
| 4 | XL(NC) | Touch panel LIFT Glass Terminal | A/D |
| 5 | YU(NC) | Touch panel Top Film Terminal | A/D |
| 6 | IOVCC | Supply voltage for IO (1.8-3.3V). | P |
| 7 | IOVCC | Supply voltage for IO (1.8-3.3V). | P |
| 8 | VCI | Supply voltage (3.3V). | P |
| 9 | VCI | Supply voltage (3.3V). | P |
| 10 | IM2 | MPU Parallel interface bus and serial interface select. If use RGB Interface must select serial interface. Fix this pin at IOVCC and GND. | I |
| 11 | IM1 | | |
| 12 | IM0 | | |
| 13 | RESET | This signal will reset the device and must be applied to properly initialize the chip. | I |
| 14 | CS | Chip select input pin ("Low" enable). Fix this pin at IOVCC or GND when not in use. | I |
| 15 | RS(SPI-SCL) | This pin is used to select "Data or Command" in the parallel interface. When D/CX = '1', data is selected. When D/CX = '0', command is selected. This pin is used serial interface clock in 3-wire 9-bit / 4-wire 8-bit serial data interface. Fix this pin at IOVCC or GND when not in use. | I |
| 16 | WR(SPI-RS) | The data is applied on the rising edge of the SCL signal. Fix this pin at IOVCC or GND when not in use. | I |
| 17 | RD | Serves as a read signal and MCU read data at the rising edge. Fix this pin at IOVCC or GND when not in use. | I |



| | | | |
|-------|---------|--|-----|
| 18 | VSYNC | Frame synchronizing signal for RGB interface operation. Fix this pin at IOVCC or GND when not in use. | I |
| 19 | HSY NC | Line synchronizing signal for RGB interface operation. Fix this pin at IOVCC or GND when not in use. | I |
| 20 | ENABLE | Data enable signal for RGB interface operation. Fix this pin at IOVCC or GND when not in use. | I |
| 21 | DOTCLK | Dot clock signal for RGB interface operation. Fix this pin at IOVCC or GND when not in use. | I |
| 22 | SDA | Serial input signal. The data is applied on the rising edge of the SCL signal. If not used, fix this pin at IOVCC or GND. | I |
| 23-40 | DB0-DB7 | Data bus. If not used pin, fix this pin to GND. | I/O |
| 41 | SDO | SPI interface output pin. -The data is output on the falling edge of the SCL signal. -If not used, let this pin open. | O |
| 42 | GND | Ground. | P |
| 43 | LEDA | Anode pin of backlight | P |
| 44 | LEDK1 | Cathode pin OF backlight | P |
| 45 | LEDK2 | Cathode pin OF backlight | P |
| 46 | LEDK3 | Cathode pin OF backlight | P |
| 47 | LEDK4 | Cathode pin OF backlight | P |
| 48 | LEDK5 | Cathode pin OF backlight | P |
| 49 | LEDK6 | Cathode pin OF backlight | P |
| 50 | GND | Ground. | P |



LCD Optical Characteristics

Optical specification

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Note |
|--------------------------------------|-------------|--|---------|---------|---------|------|---|
| Transmittance (with Polarizer) | T (%) | $\Theta=0$ Normal viewing angle | — | (4.63) | — | % | Measuring with Polarizer , Reference Only |
| Transmittance (without Polarizer) | T (%) | | — | (17.5) | — | % | |
| Contrast Ratio | CR | | 600 | 800 | — | — | (1)(2) |
| Response Time | $T_R + T_F$ | | — | 30 | 40 | msec | (1)(3) |
| Color gamut | (%) | | — | 60 | — | % | C-light |
| Color chromaticity (CIE1931) | White | W_x | (0.288) | (0.308) | (0.328) | — | (1)(4) CF glass |
| | | W_y | (0.310) | (0.330) | (0.350) | — | |
| | Red | R_x | (0.621) | (0.641) | (0.661) | — | |
| | | R_y | (0.317) | (0.337) | (0.357) | — | |
| | Green | G_x | (0.254) | (0.274) | (0.294) | — | |
| | | G_y | (0.540) | (0.560) | (0.580) | — | |
| | Blue | B_x | (0.121) | (0.141) | (0.161) | — | |
| | | B_y | (0.093) | (0.113) | (0.133) | — | |
| Viewing angle | Hor. | Θ_L | — | 80 | — | — | (1)(4) Measuring with Polarizer , Reference Only |
| | | Θ_R | — | 80 | — | | |
| | Ver. | Θ_U | — | 80 | — | | |
| | | Θ_D | — | 80 | — | | |
| Optima View Direction | Free | | | | | | (5) |



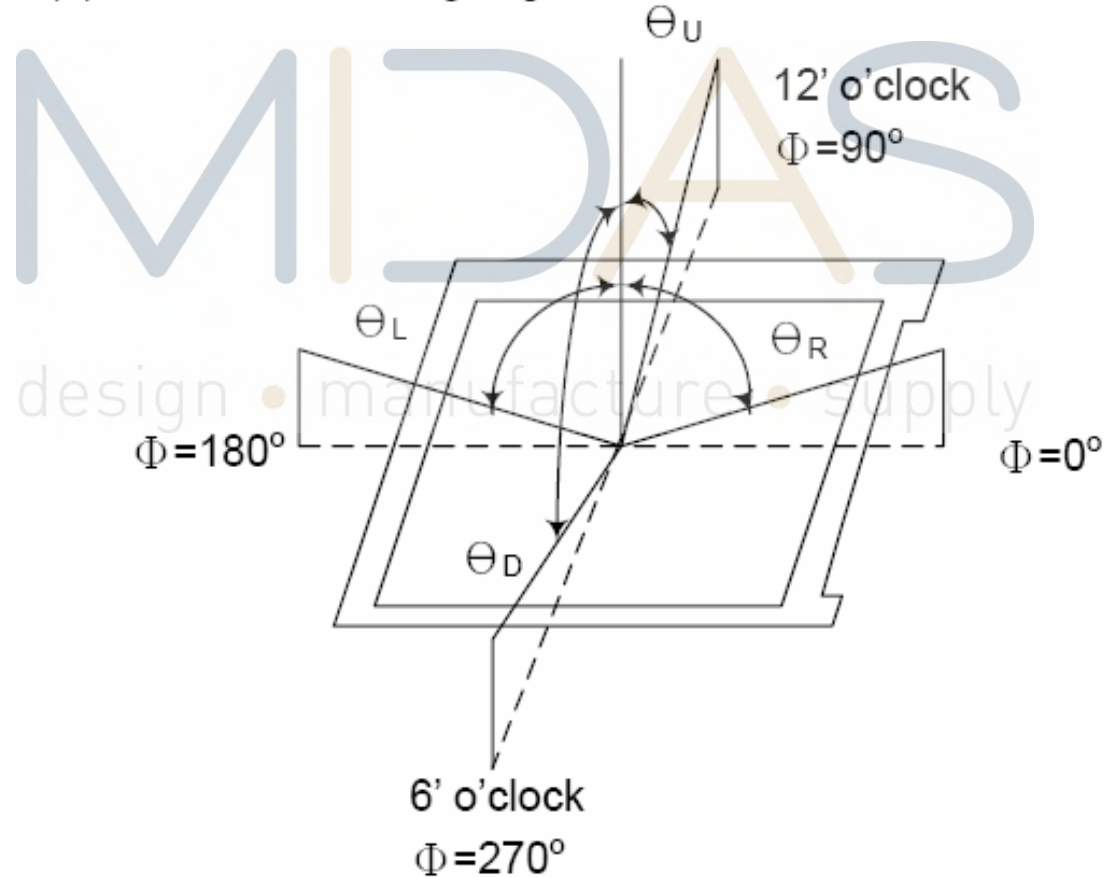
Measuring Condition

- Measuring surrounding: dark room
- Ambient temperature: $25\pm 2^{\circ}\text{C}$
- 15min. warm-up time.

Measuring Equipment

- FPM520 of Midas, which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

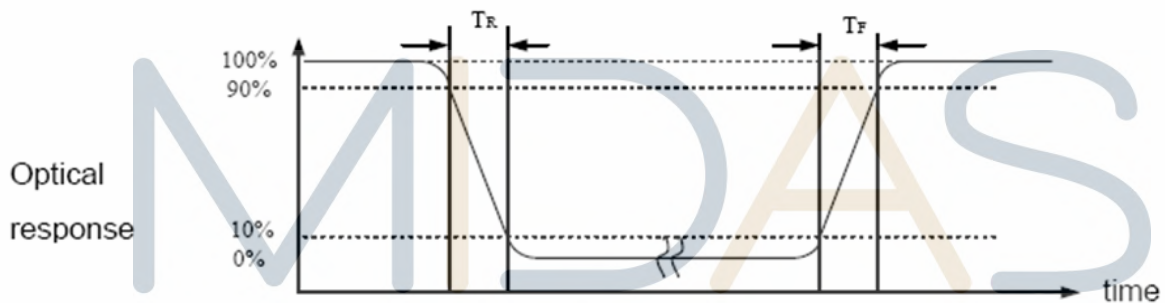
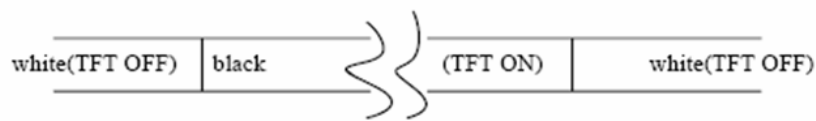
Note (1) Definition of Viewing Angle:



Note (2) Definition of Contrast Ratio (CR) :
measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note (3) Definition of Response Time : Sum of T_R and T_F



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Electrical Characteristics

Absolute Maximum Rating (Ta=25 VSS=0V)

| Characteristics | Symbol | Min. | Max. | Unit |
|----------------------------------|---------------------|------|------|------|
| Digital Supply Voltage | VDD -0.3 | | 4.6 | V |
| Digital interface supply Voltage | VDDIO | -0.3 | 4.6 | V |
| Operating temperature | T _{OP} -20 | | +70 | °C |
| Storage temperature | T _{ST} -30 | | +80 | °C |

DC Electrical Characteristics

| Characteristics | Symbol | Min. | Typ. | Max. | Unit | Note |
|----------------------------------|--------------------------------------|------|------|----------------------|------|------|
| Digital Supply Voltage | VDD 2.4 | | 3.3 | 4.2 | V | |
| Digital interface supply Voltage | VDDIO 1.65 | | 3.3 | 4.2 | V | |
| Normal mode Current consumption | I _{DD} -- | | 8 | -- | mA | |
| Level input voltage | V _{IH} 0.7V _{DDIO} | | | VDDIO | V | |
| | V _{IL} GND | | | 0.3V _{DDIO} | V | |
| Level output voltage | V _{OH} 0.8V _{DDIO} | | | VDDIO | V | |
| | V _{OL} GND | | | 0.2V _{DDIO} | V | |

LED Backlight Characteristics

The back-light system is edge-lighting type with 6 chips White LED

| Item | Symbol | Min. | Typ. | Max. | Unit | Note |
|-----------------|--------------------|------|------|------|-------------------|----------|
| Forward Current | I _F 90 | | 120 | -- | mA | |
| Forward Voltage | V _F -- | | 3.2 | -- | V | |
| LCM Luminance | L _V 450 | | 500 | -- | cd/m ² | IF=120mA |



| | | | | | | |
|---------------|-----|-------|----|----|------|---------|
| LED life time | Hr | 50000 | -- | -- | Hour | Note1,2 |
| Uniformity | AVg | 80 | -- | -- | % | |

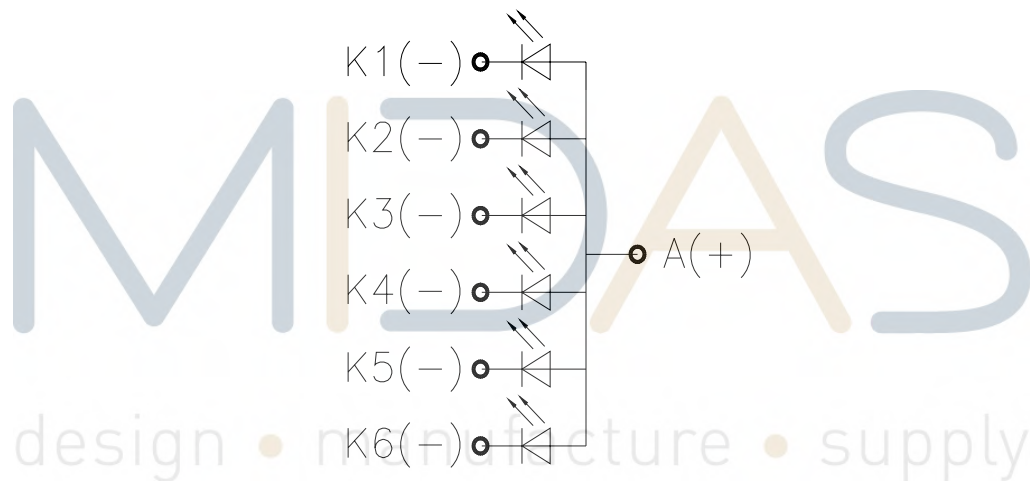
Note (1) LED life time (Hr) can be defined as the time in which it continues to operate under the condition:

$T_a=25\pm 3\text{ }^\circ\text{C}$, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note (2) The "LED life time" is defined as the module brightness decrease to 50% original brightness at

$T_a=25\text{ }^\circ\text{C}$ and $I_L=120\text{mA}$. The LED lifetime could be decreased if operating I_L is larger than 120mA.

The constant current driving method is suggested.

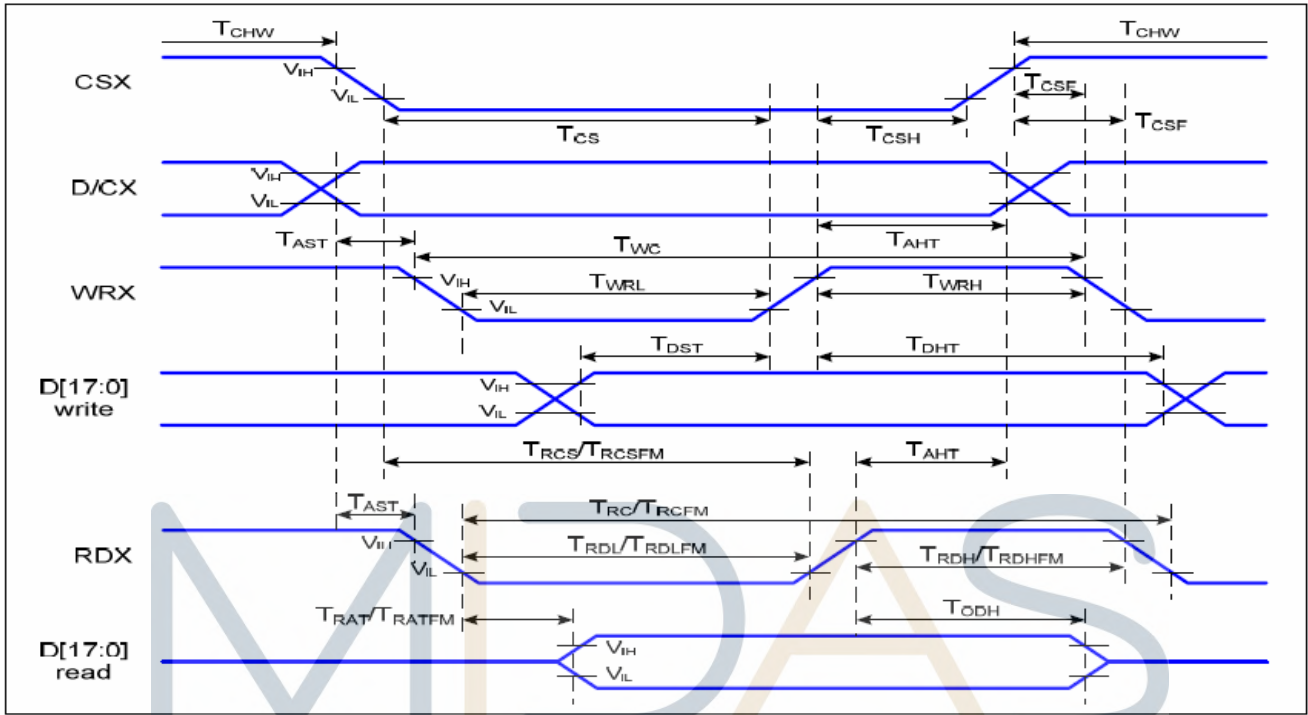


BLU CIRCUIT DIAGRAM



AC Characteristic

8080 Series MCU Parallel Interface Timing Characteristics: 18/16/9/8-bit Bus



VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta= -30 to 70 °C

| Signal | Symbol | Parameter | Min | Max | Unit | Description |
|----------|-------------|------------------------------------|-----|-----|------|-----------------------------|
| D/CX | T_{AST} | Address setup time | 0 | | ns | - |
| | T_{AHT} | Address hold time (Write/Read) | 10 | | ns | - |
| CSX | T_{CHW} | Chip select "H" pulse width | 0 | | ns | - |
| | T_{CS} | Chip select setup time (Write) | 15 | | ns | - |
| | T_{RCS} | Chip select setup time (Read ID) | 45 | | ns | - |
| | T_{RCSFM} | Chip select setup time (Read FM) | 355 | | ns | - |
| | T_{CSF} | Chip select wait time (Write/Read) | 10 | | ns | - |
| | T_{CSH} | Chip select hold time | 10 | | ns | - |
| WRX | T_{WC} | Write cycle | 66 | | ns | - |
| | T_{WRH} | Control pulse "H" duration | 15 | | ns | - |
| | T_{WRL} | Control pulse "L" duration | 15 | | ns | - |
| RDX (ID) | T_{RC} | Read cycle (ID) | 160 | | ns | When read ID data |
| | T_{RDH} | Control pulse "H" duration (ID) | 90 | | ns | |
| | T_{RDL} | Control pulse "L" duration (ID) | 45 | | ns | |
| RDX (FM) | T_{RCFM} | Read cycle (FM) | 450 | | ns | When read from frame memory |
| | T_{RDHFM} | Control pulse "H" duration (FM) | 90 | | ns | |
| | T_{RDLFM} | Control pulse "L" duration (FM) | 355 | | ns | |
| D[17:0] | T_{DST} | Data setup time | 10 | | ns | For CL=30pF |



| | | | | | |
|--|-------------|-----------------------|----|-----|----|
| | T_{DHT} | Data hold time | 10 | | ns |
| | T_{RAT} | Read access time (ID) | | 40 | ns |
| | T_{RATFM} | Read access time (FM) | | 340 | ns |
| | T_{ODH} | Output disable time | 20 | 80 | ns |

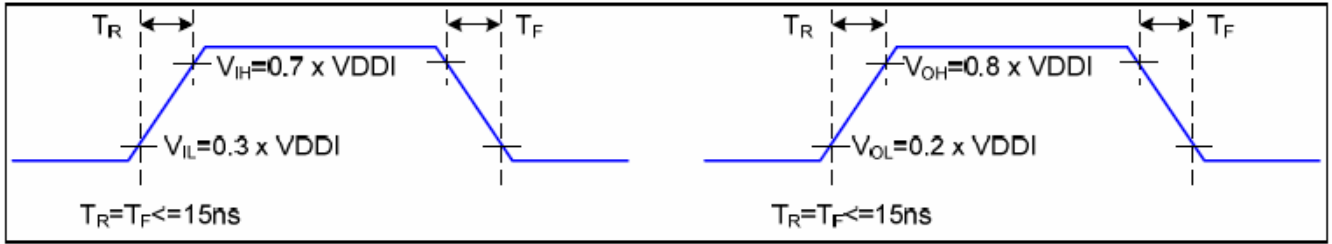


Figure 2 Rising and Falling Timing for I/O Signal

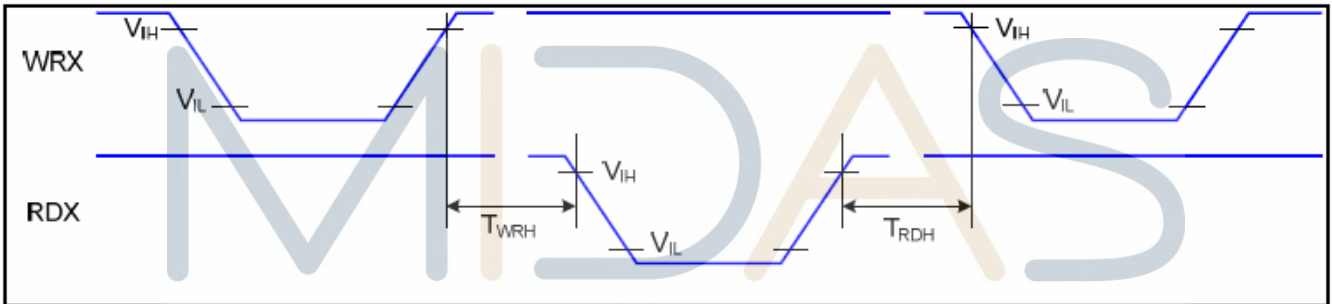
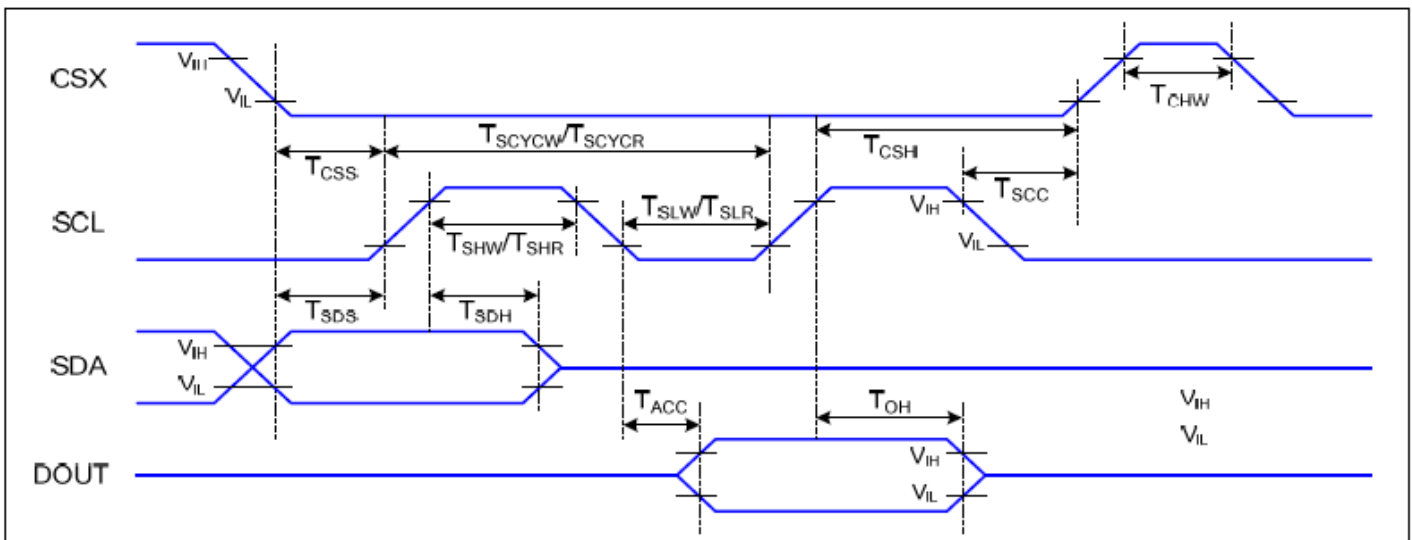


Figure 3 Write-to-Read and Read-to-Write Timing

Note: The rising time and falling time (T_r , T_f) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Display Serial Interface Timing Characteristics (3-line SPI system)

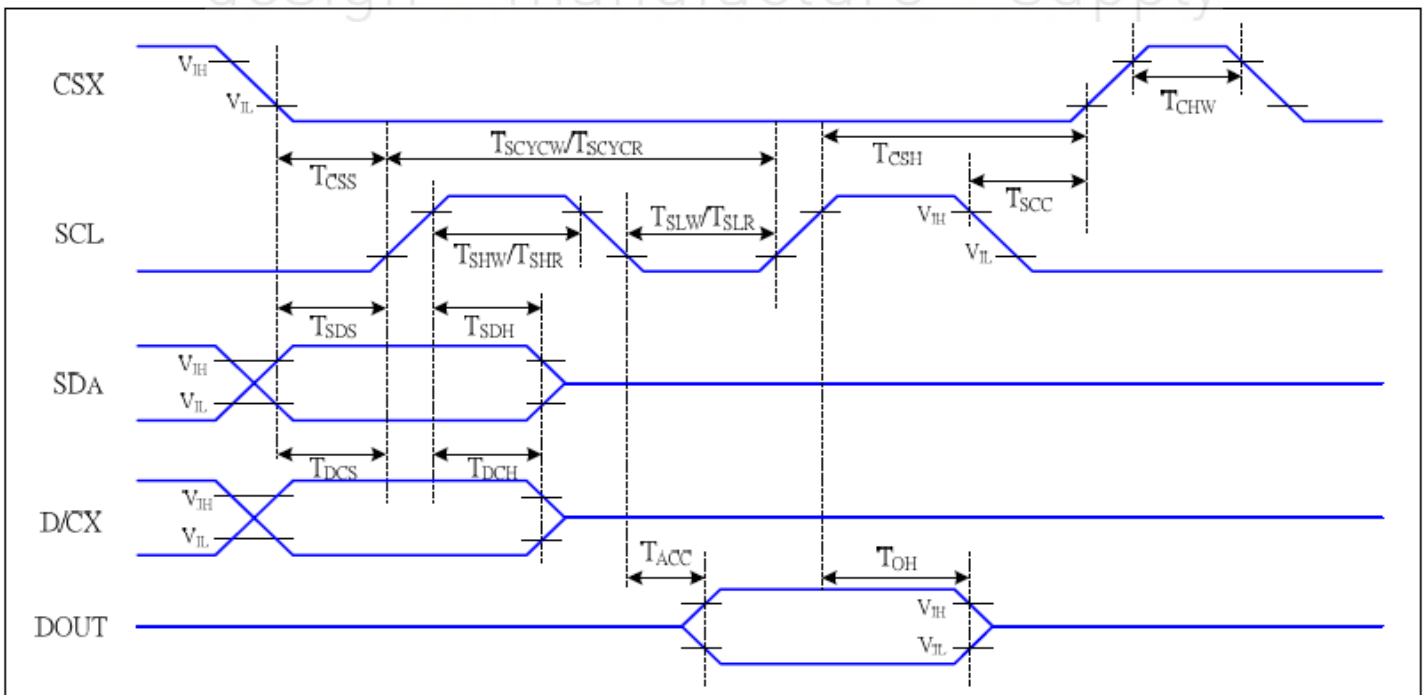


VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 to 70 °C

| Signal | Symbol | Parameter | Min | Max | Unit | Description |
|--------------|-------------|--------------------------------|-----|-----|------|---------------------|
| CSX | T_{CSS} | Chip select setup time (write) | 15 | | ns | |
| | T_{CSH} | Chip select hold time (write) | 15 | | ns | |
| | T_{CSS} | Chip select setup time (read) | 60 | | ns | |
| | T_{SCC} | Chip select hold time (read) | 65 | | ns | |
| | T_{CHW} | Chip select "H" pulse width | 40 | | ns | |
| SCL | T_{SCYCW} | Serial clock cycle (Write) | 66 | | ns | |
| | T_{SHW} | SCL "H" pulse width (Write) | 15 | | ns | |
| | T_{SLW} | SCL "L" pulse width (Write) | 15 | | ns | |
| | T_{SCYCR} | Serial clock cycle (Read) | 150 | | ns | |
| | T_{SHR} | SCL "H" pulse width (Read) | 60 | | ns | |
| | T_{SLR} | SCL "L" pulse width (Read) | 60 | | ns | |
| SDA (DIN) | T_{SDS} | Data setup time | 10 | | ns | |
| | T_{SDH} | Data hold time | 10 | | ns | |
| DOUT | T_{ACC} | Access time | 10 | 50 | ns | For maximum CL=30pF |
| | T_{OH} | Output disable time | 15 | 50 | ns | For minimum CL=8pF |

Display Serial Interface Timing Characteristics (4-line SPI system)

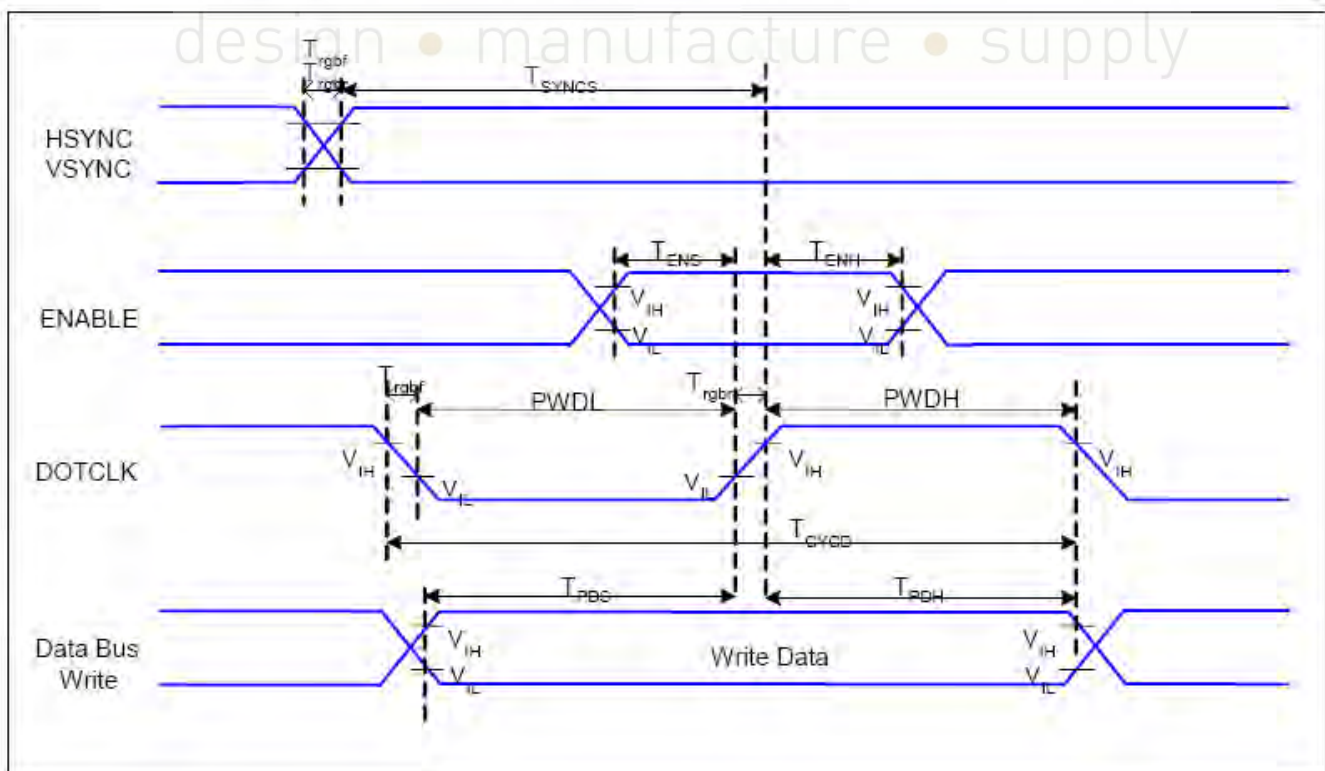
design • manufacture • supply



VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 to 70 °C

| Signal | Symbol | Parameter | MIN | MAX | Unit | Description |
|-----------|--------------------|--------------------------------|-----|-----|------|---------------------------|
| CSX | T _{CSS} | Chip select setup time (write) | 15 | | ns | |
| | T _{CSH} | Chip select hold time (write) | 15 | | ns | |
| | T _{CSS} | Chip select setup time (read) | 60 | | ns | |
| | T _{SCC} | Chip select hold time (read) | 65 | | ns | |
| | T _{CHW} | Chip select "H" pulse width | 40 | | ns | |
| SCL | T _{SCYCW} | Serial clock cycle (Write) | 66 | | ns | -write command & data ram |
| | T _{SHW} | SCL "H" pulse width (Write) | 15 | | ns | |
| | T _{SLW} | SCL "L" pulse width (Write) | 15 | | ns | |
| | T _{SCYCR} | Serial clock cycle (Read) | 150 | | ns | -read command & data ram |
| | T _{SHR} | SCL "H" pulse width (Read) | 60 | | ns | |
| | T _{SLR} | SCL "L" pulse width (Read) | 60 | | ns | |
| D/CX | T _{DCS} | D/CX setup time | 10 | | ns | |
| | T _{DCH} | D/CX hold time | 10 | | ns | |
| SDA (DIN) | T _{SDS} | Data setup time | 10 | | ns | |
| | T _{SDH} | Data hold time | 10 | | ns | |
| DOUT | T _{ACC} | Access time | 10 | 50 | ns | For maximum CL=30pF |
| | T _{OH} | Output disable time | 15 | 50 | ns | For minimum CL=8pF |

Parallel RGB Interface Timing Characteristics



VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 ~ 70 °C

| Signal | Symbol | Parameter | MIN | MAX | Unit | Description |
|--------------|--------------------|-------------------------------|-----|-----|------|-------------|
| HSYNC, VSYNC | T _{SYNCS} | VSYNC, HSYNC Setup Time | 30 | - | ns | |
| ENABLE | T _{ENS} | Enable Setup Time | 25 | - | ns | |
| | T _{ENH} | Enable Hold Time | 25 | - | ns | |
| DOTCLK | PWDH | DOTCLK High-level Pulse Width | 60 | - | ns | |
| | PWDL | DOTCLK Low-level Pulse Width | 60 | - | ns | |
| | T _{CYCD} | DOTCLK Cycle Time | 120 | - | ns | |
| | Trghr, Trghf | DOTCLK Rise/Fall time | - | 20 | ns | |
| DB | T _{PDS} | PD Data Setup Time | 50 | - | ns | |
| | T _{PDH} | PD Data Hold Time | 50 | - | ns | |

| Parameters | Symbols | Condition | Min. | Typ. | Max. | Units |
|----------------------------|---------|-----------|------|------|------|--------|
| Horizontal Synchronization | Hsync | | 2 | 10 | 16 | DOTCLK |
| Horizontal Back Porch | HBP | | 2 | 20 | 24 | DOTCLK |
| Horizontal Address | HAdr | | - | 240 | - | DOTCLK |
| Horizontal Front Porch | HFP | | 2 | 10 | 16 | DOTCLK |
| Vertical Synchronization | Vsync | | 1 | 2 | 4 | Line |
| Vertical Back Porch | VBP | | 1 | 2 | - | Line |
| Vertical Address | VAdr | | - | 320 | - | Line |
| Vertical Front Porch | VFP | | 3 | 4 | - | Line |

Setting Example: To set frame frequency to 70Hz:

Internal Clock

Internal Oscillation Clock: 615KHz

DIV[1:0] = 2'b0 (x 1/1)

RTN[4:0] = 5'h1b (27 clocks)

FP = 7'h2 (2 lines), BP = 7'h2 (2 lines), NL = 6'h27 (320 lines)

Frame Rate → 70.30Hz



DOTCLK

HSYNC = 10 CLK

HBP = 20 CLK

HFP=10 CLK

70Hz x (2 + 320 + 2) lines x (10 + 20 + 240 + 10) clocks = 6.35MHz

DOTCLK frequency = 6.35MHz

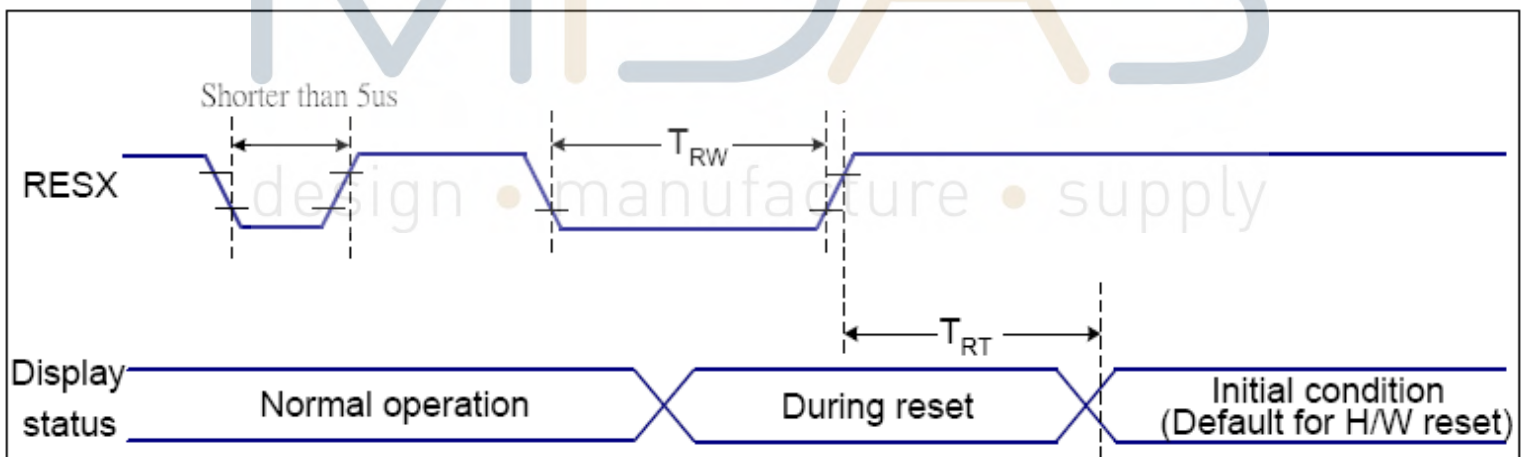
6.35 MHz / 615KHz = 10.32 □ Set PCDIV so that PCLK is divided by 10.

external fosc = 6.35 MHz / 10 = 635KHz

PCDIV = [6.35MHz / 635KHz) / 2] - 1 = 4

PCDIV[5:0] = 6'h04 (10 DOTCLK)

Reset Timing Characteristics



VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 ~ 70 °C

| Related Pins | Symbol | Parameter | MIN | MAX | Unit |
|--------------|--------|----------------------|--------------------|---------------|------|
| RESX | TRW | Reset pulse duration | 10 | - | us |
| | TRT | Reset cancel | - | 5 (Note 1, 5) | ms |
| - | | | 120 (Note 1, 6, 7) | ms | |

Notes:

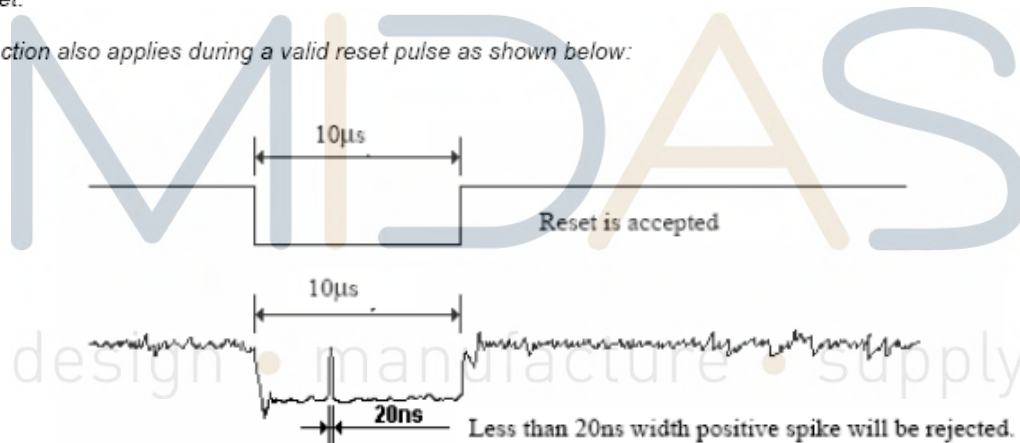
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

| RESX Pulse | Action |
|---------------------|----------------|
| Shorter than 5us | Reset Rejected |
| Longer than 9us | Reset |
| Between 5us and 9us | Reset starts |

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.



LCD Module Out-Going Quality Level

VISUAL & FUNCTION INSPECTION STANDARD

Inspection conditions

Inspection performed under the following conditions is recommended.

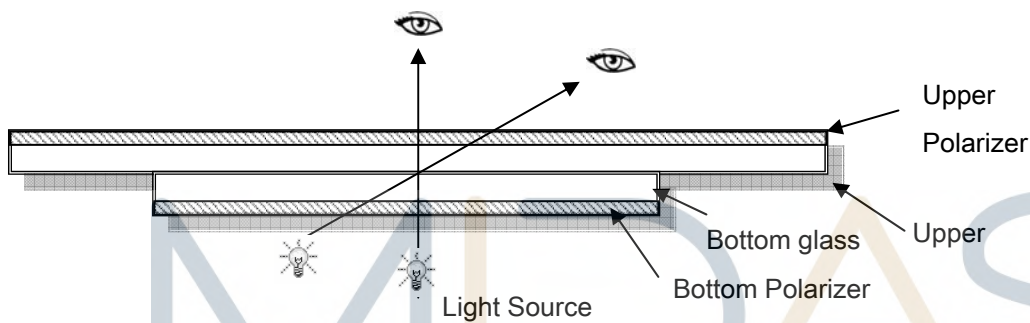
Temperature : $25\pm 5^{\circ}\text{C}$

Humidity : $65\%\pm 10\%\text{RH}$

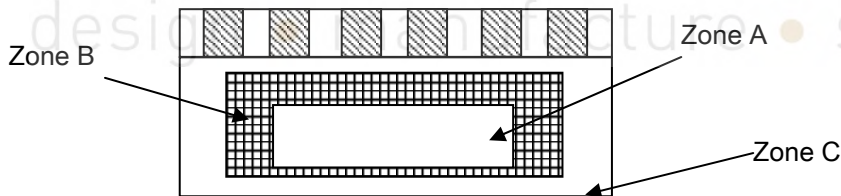
Viewing Angle : Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance:30-50cm



Definition



Zone A : Effective Viewing Area(Character or Digit can be seen)

Zone B : Viewing Area except Zone A

Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer .)

Note:

As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer.

Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class II

AQL:

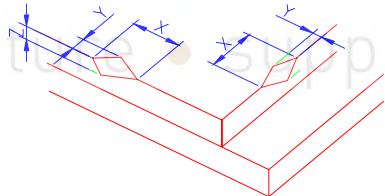


| | |
|--------------|--------------|
| Major defect | Minor defect |
| 0.65 1.5 | |

LCD: Liquid Crystal Display , TP: Touch Panel , LCM: Liquid Crystal Module

| No | Items to be inspected | Criteria | Classification of defects |
|----|-----------------------|---|---------------------------|
| 1 | Functional defects | 1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. 4) TP no function | Major |
| 2 | Missing | Missing component | |
| 3 | Outline dimension | Overall outline dimension beyond the drawing is not allowed | |
| 4 | Color tone | Color unevenness, refer to limited sample | Minor |
| 5 | Soldering appearance | Good soldering , Peeling off is not allowed. | |
| 6 | LCD/Polarizer/TP | Black/White spot/line, scratch, crack, etc. | |

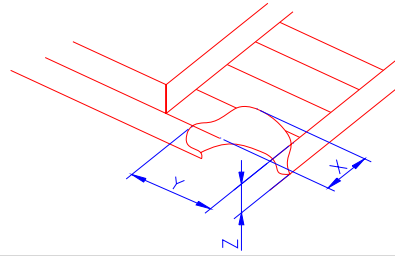
Criteria (Visual)

| Number Items | Criteria(mm) | | | | | | |
|--------------------------------|--|-----|--|---|--------|--------------------------------|----|
| 1.0 LCD Crack/Broken |  <p>(1) The edge of LCD broken</p> <table border="1" data-bbox="842 1462 1374 1617"> <thead> <tr> <th>X Y</th> <th></th> <th>Z</th> </tr> </thead> <tbody> <tr> <td>≤3.0mm</td> <td><Inner border line of the seal</td> <td>≤T</td> </tr> </tbody> </table> | X Y | | Z | ≤3.0mm | <Inner border line of the seal | ≤T |
| X Y | | Z | | | | | |
| ≤3.0mm | <Inner border line of the seal | ≤T | | | | | |
| NOTE: X: Length Y: Width | | | | | | | |



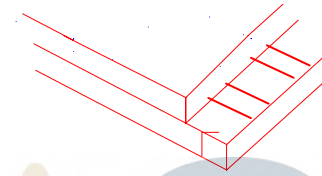
Z: Height
 L: Length of ITO,
 T: Height of LCD

(2) LCD corner broken



| | | |
|--------|----|----|
| X Y | | Z |
| ≤3.0mm | ≤L | ≤T |

(3) LCD crack



Crack
 Not allowed

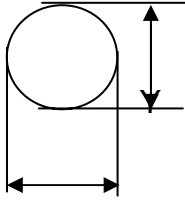
MIDAS

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2.0

Spot defect



X

$\Phi=(X+Y)/2$

① light dot (LCD/TP/Polarizer black/white spot, light dot, pinhole, dent, stain)

| Zone Size (mm) | Acceptable Qty | | |
|-------------------------|----------------------------------|---|---|
| | A | B | C |
| $\Phi \leq 0.10$ | Ignore | | |
| $0.10 < \Phi \leq 0.15$ | 3 (distance $\geq 10\text{mm}$) | | |
| $0.15 < \Phi \leq 0.2$ | 1 | | |
| $0.2 < \Phi$ | 0 | | |

② Dim spot (LCD/TP/Polarizer dim dot, light leakage, dark spot)

| Zone Size (mm) | Acceptable Qty | | |
|-----------------------|----------------------------------|---|---|
| | A | B | C |
| $\Phi \leq 0.1$ | Ignore | | |
| $0.1 < \Phi \leq 0.2$ | 2 (distance $\geq 10\text{mm}$) | | |
| $0.2 < \Phi \leq 0.3$ | 1 | | |
| $\Phi > 0.3$ | 0 | | |

③ Polarizer accidented spot

| Zone Size (mm) | Acceptable Qty | | |
|-----------------------|----------------------------------|---|---|
| | A | B | C |
| $\Phi \leq 0.2$ | Ignore | | |
| $0.2 < \Phi \leq 0.5$ | 2 (distance $\geq 10\text{mm}$) | | |
| $\Phi > 0.5$ | 0 | | |

Line defect (LCD/TP/Polarizer black/white line, scratch, stain)

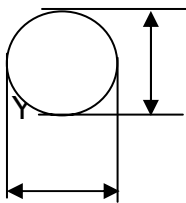
| Width(mm) Length(mm) | Acceptable Qty | | |
|------------------------|-----------------------|----------|--------|
| | A | B | C |
| $\Phi \leq 0.03$ | Ignore | | |
| $0.03 < W \leq 0.05$ L | ≤ 3.0 N | ≤ 2 | Ignore |
| $0.05 < W \leq 0.08$ L | ≤ 2.0 N | ≤ 2 | |
| $0.08 < W$ | Define as spot defect | | |



Items Criteria

(mm)

Spot defect



X

$\Phi=(X+Y)/2$

① light dot (LCD/TP/Polarizer black/white spot, light dot, pinhole, dent, stain)

| Zone Size (mm) | Acceptable Qty | | |
|--------------------------|----------------------------------|---|--------|
| | A | B | C |
| $\Phi \leq 0.10$ Ignore | | | Ignore |
| $0.10 < \Phi \leq 0.15$ | 3(distance $\geq 10\text{mm}$) | | |
| $0.15 < \Phi \leq 0.2$ 1 | | | |
| $0.2 < \Phi$ 0 | | | |

② Dim spot (LCD/TP/Polarizer dim dot, light leakage, dark spot)

| Zone Size (mm) | Acceptable Qty | | |
|-------------------------|----------------------------------|---|--------|
| | A | B | C |
| $\Phi \leq 0.1$ Ignore | | | Ignore |
| $0.1 < \Phi \leq 0.2$ | 2(distance $\geq 10\text{mm}$) | | |
| $0.2 < \Phi \leq 0.3$ 1 | | | |
| $\Phi > 0.3$ | 0 | | |

③ Polarizer accidented spot

| Zone Size (mm) | Acceptable Qty | | |
|------------------------|----------------------------------|---|--------|
| | A | B | C |
| $\Phi \leq 0.2$ Ignore | | | Ignore |
| $0.2 < \Phi \leq 0.5$ | 2(distance $\geq 10\text{mm}$) | | |
| $\Phi > 0.5$ 0 | | | |



Line defect
(LCD/TP
/Polarizer
black/white
line,
scratch,
stain)

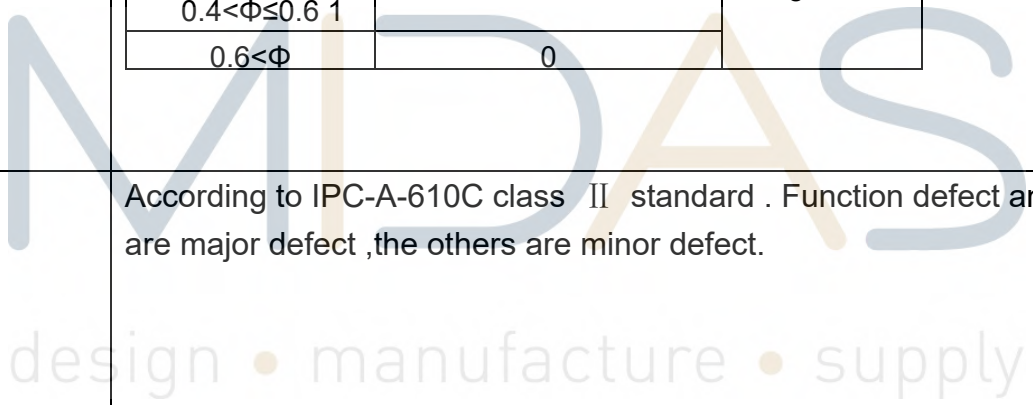
| Width(mm) | ength(mm) | Acceptable Qty | | |
|----------------------|-----------------------|----------------|---|--------|
| | | A | B | C |
| $\Phi \leq 0.03$ | Ignore | Ignore | | Ignore |
| $0.03 < W \leq 0.05$ | ≤ 3.0 N | ≤ 2 | | |
| $0.05 < W \leq 0.08$ | ≤ 2.0 N | ≤ 2 | | |
| $0.08 < W$ | Define as spot defect | | | |

Polarizer
Bubble

| Z one Size (mm) | Acceptable Qty | | |
|-----------------------|---------------------------|---|--------|
| | A | B | C |
| $\Phi \leq 0.2$ | Ignore | | Ignore |
| $0.2 < \Phi \leq 0.4$ | 2 (distance ≥ 10 mm) | | |
| $0.4 < \Phi \leq 0.6$ | 1 | | |
| $0.6 < \Phi$ | 0 | | |

SMT

According to IPC-A-610C class II standard . Function defect and missing part are major defect ,the others are minor defect.



TP bubble/
accidented
spot

| Size Φ (mm) | Acceptable Qty | | |
|-----------------------|-----------------------------|---|--------|
| | A | B | C |
| $\Phi \leq 0.1$ | Ignore | | Ignore |
| $0.1 < \Phi \leq 0.2$ | 2 (distance ≥ 10 mm) | | |
| $0.2 < \Phi \leq 0.3$ | 1 | | |
| $0.3 < \Phi$ | 0 | | |

Assembly
deflection

beyond the edge of backlight ≤ 0.15 mm



5.0

TP
Related

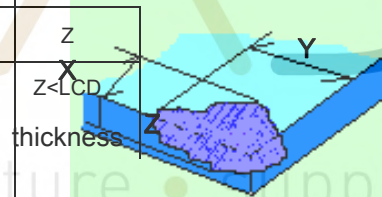
Newton
Ring

Newton Ring area > 1/3
TP area NG
Newton Ring area ≤ 1/3
TP area OK



TP corner
broken
X: length
Y: width
Z: height

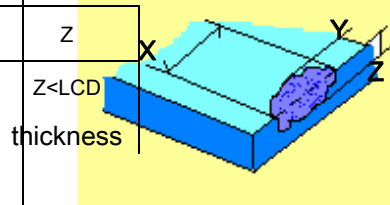
| X | Y |
|-----------------------|-----------------------|
| $X \leq 3.0\text{mm}$ | $Y \leq 3.0\text{mm}$ |



*
Circuitry broken is not
allowed.

TP edge
broken
X: length
Y: width
Z: height

| X | Y |
|-----------------------|-----------------------|
| $X \leq 6.0\text{mm}$ | $Y \leq 2.0\text{mm}$ |



* Circuitry broken is
not allowed.



Criteria (functional items)

| Number | Items | Criteria (mm) |
|--------|-----------------------|---------------|
| 1 | No display | Not allowed |
| 2 | Missing segment | Not allowed |
| 3 | Short | Not allowed |
| 4 | Backlight no lighting | Not allowed |
| 5 | TP no function | Not allowed |



Reliability Test Result

Condition

| Item | Condition | Sample Size | Test Result | Note |
|--------------------------------------|-----------------------------|-------------|-------------|------|
| Low Temperature Operating Life test | -20°C, 96HR | 3ea | pass | - |
| Thermal Humidity Operating Life test | 70°C90%RH, 96HR | 3ea | pass | - |
| Temperature Cycle ON/OFF test | -20°C ↔ 70°C, ON/OFF, 20CYC | 3ea | pass | (1) |
| High Temperature | 80°C, 96HR | 3ea | pass | - |



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| | | | | |
|------------------------------|---|------|------|---|
| Storage test | | | | |
| Low Temperature Storage test | - 30°C, 96HR | 3ea | pass | - |
| ESD test | 150pF, 330Ω , ±6KV(Contact)/± 8KV(Air), 5 points/panel, 10 times/point | 3ea | pass | |
| Thermal Shock Resistance | The sample should be allowed to stand the following 5 cycles of operation: TSTL for 30 minutes -> normal temperature for 5 minutes -> TSTH for 30 minutes -> normal temperature for 5 minutes, as one cycle, then taking it out and drying it at normal temperature, and allowing it stand for 24 hours | 3ea | pass | |
| Box Drop Test | 1 Corner 3 Edges 6 faces, 66cm(MEDIUM BOX) | 1box | pass | - |

Note (1) ON Time over 10 seconds, OFF Time under 10 seconds

Cautions and Handling Precautions

Handling and Operating the Module

- (1) When the module is assembled, it should be attached to the system firmly.
Do not warp or twist the module during assembly work.
- (2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
- (3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
- (4) Do not allow drops of water or chemicals to remain on the display surface.
If you have the droplets for a long time, staining and discoloration may occur.
- (5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
- (6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.
Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with



hands, legs, or clothes, it must be washed away thoroughly with soap.

- (8) Protect the module from static; it may cause damage to the CMOS ICs.
- (9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (10) Do not disassemble the module.
- (11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
- (12) Pins of I/F connector shall not be touched directly with bare hands.
- (13) Do not connect, disconnect the module in the "Power ON" condition.
- (14) Power supply should always be turned on/off by the item 6.1 Power On Sequence & 6.2 Power Off Sequence

Storage and Transportation.

- (1) Do not leave the panel in high temperature, and high humidity for a long time.

It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%

- (2) Do not store the TFT-LCD module in direct sunlight.
- (3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
- (4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.
In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
- (5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

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