DATASHEET

Product Description

This specification defines the electrical and mechanical requirements for 260 pin, 1.2 V (VDD), Double Data Rate, Synchronous DRAM Dual In-Line Memory Modules (DDR4 SDRAM SO-DIMM). These DDR4 SO-DIMMs are intended for use as main memory when installed in PCs, laptops and other systems.

Reference design examples are included which provide an initial basis for DDR4 SO-DIMM designs. Modifications to these reference designs may be required to meet all system timing, signal integrity and thermal requirements for DDR4-2400 support. All DDR4 SO-DIMM implementations must use simulations and lab verification to ensure proper timing requirement and signal integrity in the design.

Features:

- JEDEC standard
- VDD= VDDQ = 1.2V±0.06V (1.14V~1.26V)
- VPP = 2.5V (2.375V to 2.75V)
- Programmable CAS Latency(posted CAS): 9,11,12,13,14,15,16,17,18
- 8-bit pre-fetch
- 16 Banks (4 Bank Groups)
- Internal(self) calibration : Internal self calibration through ZQ pin
- On Die Termination using ODT pin
- Average Refresh Period
  - 7.8us (TCASE ≤ 85°C)
  - 3.9us (85°C < TCASE < 95°C)
- DRAM operating temperature range
  - Commercial (0°C ≤ TCASE ≤ 85°C)
  - Industrial (-40°C ≤ TCASE ≤ 85°C)
- Asynchronous Reset pin supported
- Burst Length: 8 or BC4
- Package : 78 balls FBGA - x4/x8, 96 balls FBGA- x16
- POD (Pseudo Open Drain) interface for data input/output
- Serial presence detect (SPD)
- All of products are Halogen-free
- All of Lead-Free products are compliant for RoHS

Operating Temperature Condition:

Symbol	Parameter	Value	Unit	Note
T_{OPER}	Normal Operating Temperature Range	0~+85	°C	1,2,
	Extended Temperature Range	+85~+95	°C	1,3

Note: 1. Operating Temperature T_{OPER} is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2. 2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, The DRAM case temperature must be maintained between 0 - 85°C under all operating conditions. 3. Some applications require operation of the DRAM in the Extended Temperature Range between 85oC and 95oC case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:

a. Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range. Please refer to the DIMM SPD for option availability.

Specifications:

Speed	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	Unit
	11-11-11	13-13-13	15-15-15	17-17-17	
tCK(min)	1.25	1.071	0.938	0.833	ns
CAS Latency	11	13	15	17	nCK
tRCD(min)	13.75	13.92	14.06	14.16	ns
tRP(min)	13.75	13.92	14.06	14.16	ns
tRAS(min)	35	34	33	32	ns
tRC(min)	48.75	47.92	47.06	46.16	ns

AC & DC Operating Conditions:

Symbol	Parameter	Rating			Unit	NOTE
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.14	1.2	1.26	V	1,2,3
VDDQ	Supply Voltage for Output	1.14	1.2	1.26	V	1,2,3
VPP	Supply Voltage for DRAM Activating	2.375	2.5	2.75	V	3

NOTE : 1. Under all conditions VDDQ must be less than or equal to VDD.

2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

3. DC bandwidth is limited to 20MHz.

Absolute Maximum Ratings:

Symbol	Parameter	Rating	Units	NOTE
VDD	Voltage on VDD pin relative to Vss	-0.3 ~ 1.5	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3 ~ 1.5	V	1,3
VPP	Voltage on VPP pin relative to Vss	-0.3 ~ 3.0	V	4
V_{IN}, V_{OUT}	Voltage on any pin except VREFCA relative to VSS	-0.3 ~ 1.5	V	1,3,5
T_{STG}	Storage Temperature	-55 to + 100	‘C	1,2

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability 2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard. 3. VDD and VDDQ must be within 300 mV of each other at all times;and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREFCA may be equal to or less than 300 mV 4. VPP must be equal or greater than VDD/VDDQ at all times.

Pin Definition:

Pin Name	Description	Pin Name	Description
A0-A17	SDRAM address bus	SCL	Serial bus clock for SPD
BA0,BA1	SDRAM bank select	SDA	Serial bus data line for SPD
BG0,BG1	SDRAM bank group select	SA0-SA2	Slave address select for SPD
RAS_n	SDRAM row address strobe	PARITY	SDRAM parity input
CAS_n	SDRAM column address strobe	VDD	SDRAM I/O and core power supply
WE_n	SDRAM write enable	12V	Optional power supply on socket but not used on UDIMM
CS0_n,CS1_n	DIMM Rank Select Lines	VREFCA	
CKE0,CKE1	SDRAM clock enable lines	VSS	Power supply return (ground)
ODT0,ODT1	On-die termination control lines	VDDSPD	Power supply used to power the I2C bus on the SPD 2.5V or 3.3V.
ACT_n	SDRAM activate	ALERT_n	SDRAM ALERT_n
DQ0-DQ63	DIMM memory data bus	VPP	SDRAM Supply
CB0-CB7	DIMM ECC check bits	RESET_N	Set DRAMs to a Known State
TDQS0_t-DQS8_t TDQS0_c-DQS8_c	Dummy loads for mixed populations of x4 based and x8 based RDIMMs. Not used on UDIMMs	DM0_n-DM8_n DBI0_n-DBI8_n	SDRAM data masks/data bus inversion(x8-based x72 DIMMs)
DQS0_t-DQS8_t	SDRAM data strobes(positive line of differential pair)	EVENT_n	SPD signals a thermal event has occurred
DQS0_c-DQS8_c	SDRAM data strobes(negative line of differential pair)	VTT	SDRAM I/O termination supply

CK0_t, CK1_t	SDRAM clock (positive line of differential pair)	RFU	Reserved for future use
CK0_c, CK1_c	SDRAM clock (negative line of differential pair)		

NOTE :

1. Address A17 is not valid for x8 and x16 based SDRAMs. For UDIMMs this connection pin is NC.
2. RAS_n is a multiplexed function with A16.
3. CAS_n is a multiplexed function with A15.
4. WE_n is a multiplexed function with A14.

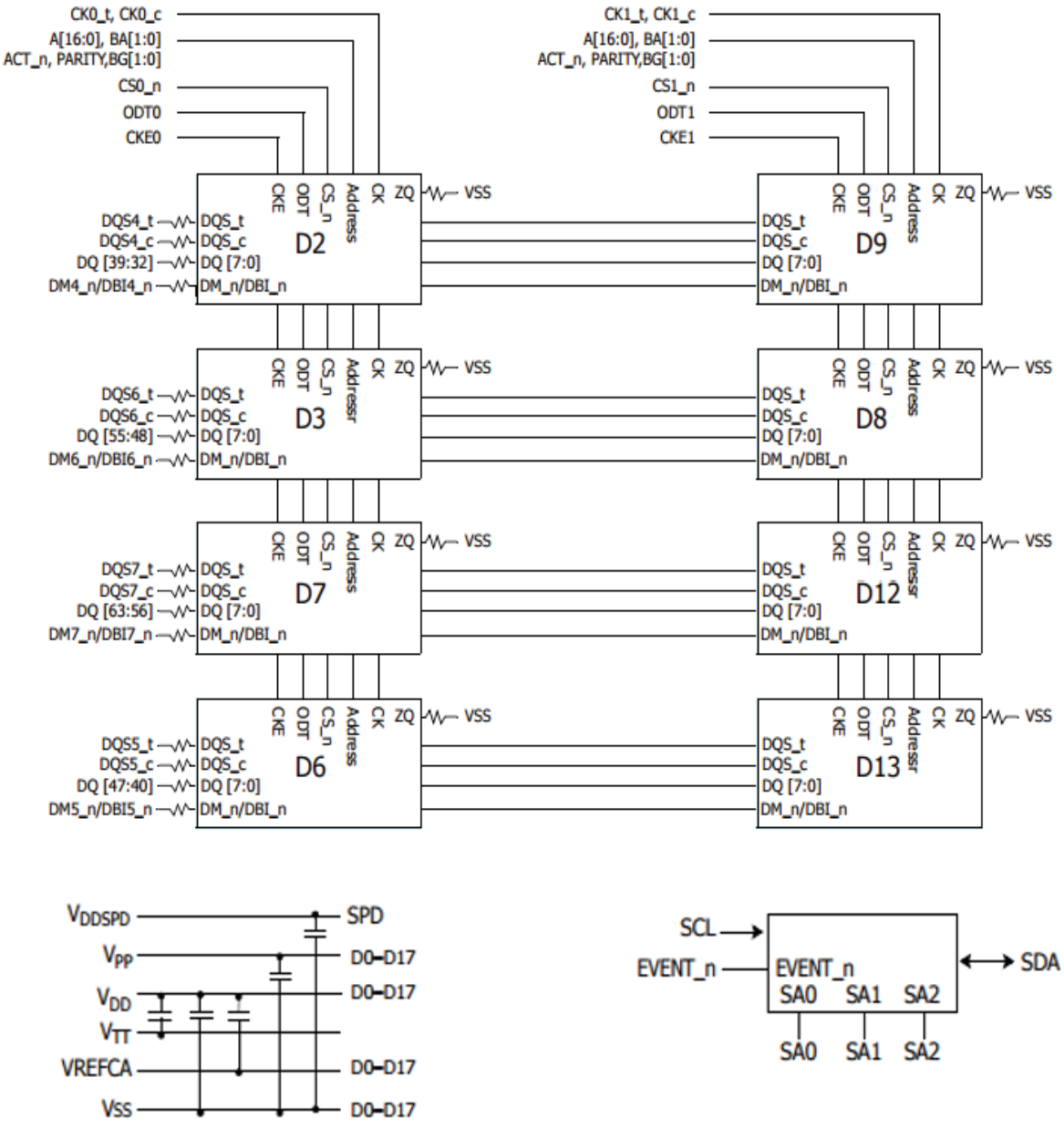
Unbuffered SO-DIMM Pin Configurations (Front/Back side):

Pin	Front Side Pin	Pin	Back Side Pin	Pin	Front Side Pin	Pin	Back Side Pin
1	VSS	2	VSS	131	A3	132	A2
3	DQ5	4	DQ4	133	A1	134	EVENT_n
5	VSS	6	VSS	135	VDD	136	VDD
7	DQ1	8	DQ0	137	CK0_t	138	CK1_t
9	VSS	10	VSS	139	CK0_c	140	CK1_c
11	DQS0_c	12	DM0_n/DBI0_n	141	VDD	142	VDD
13	DQS0_t	14	VSS	143	PARITY	144	A0
15	VSS	16	DQ6	KEY			
17	DQ7	18	VSS				
19	VSS	20	DQ2	145	BA1	146	A10/AP
21	DQ3	22	VSS	147	VDD	148	VDD
23	VSS	24	DQ12	149	CS0_n	150	BA0
25	DQ13	26	VSS	151	WE_n/A14	152	RAS_n/A16
27	VSS	28	DQ8	153	VDD	154	VDD
29	DQ9	30	VSS	155	ODT0	156	CAS_n/A15
31	VSS	32	DQS1_c	157	CS1_n	158	A13
33	DM1_n,DBI1_n	34	DQS1_t	159	VDD	160	VDD
35	VSS	36	VSS	161	ODT1	162	C0, CS2_n, NC
37	DQ15	38	DQ14	163	VDD	164	VREFCA
39	VSS	40	VSS	165	C1, CS3_n, NC	166	SA2
41	DQ10	42	DQ11	167	VSS	168	VSS
43	VSS	44	VSS	169	DQ37	170	DQ36
45	DQ21	46	DQ20	171	VSS	172	VSS
47	VSS	48	VSS	173	DQ33	174	DQ32
49	DQ17	50	DQ16	175	VSS	176	VSS

51	VSS	52	VSS	177	DQS4_c	178	DM4_n/DBI4_n
53	DQS2_c	54	DM2_n/DBI2_n	179	DQS4_t	180	VSS
55	DQS2_t	56	VSS	181	VSS	182	DQ39
57	VSS	58	DQ22	183	DQ38	184	VSS
59	DQ23	60	VSS	185	VSS	186	DQ35
61	VSS	62	DQ18	187	DQ34	188	VSS
63	DQ19	64	VSS	189	VSS	190	DQ45
65	VSS	66	DQ28	191	DQ44	192	VSS
67	DQ29	68	VSS	193	VSS	194	DQ41
69	VSS	70	DQ24	195	DQ40	196	VSS
71	DQ25	72	VSS	197	VSS	198	DQS5_c
73	VSS	74	DQS3_c	199	DM5_n,DBI5_n,	200	DQS5_t
75	DM3_n,DBI3_n,	76	DQS3_t	201	VSS	202	VSS
77	VSS	78	VSS	203	DQ46	204	DQ47
79	DQ30	80	DQ31	205	VSS	206	VSS
81	VSS	82	VSS	207	DQ42	208	DQ43
83	DQ26	84	DQ27	209	VSS	210	VSS
85	VSS	86	VSS	211	DQ52	212	DQ53
87	CB5, NC	88	CB4, NC	213	VSS	214	VSS
89	VSS	90	VSS	215	DQ49	216	DQ48
91	CB1, NC	92	CB0, NC	217	VSS	218	VSS
93	VSS	94	VSS	219	DQS6_c	220	DM6_n/DBI6_n
95	DQS8_c	96	DM8_n,DBI8_n	221	DQS6_t	222	VSS
97	DQS8_t	98	VSS	223	VSS	224	DQ54
99	VSS	100	CB6, NC	225	DQ55	226	VSS
101	CB2, NC	102	VSS	227	VSS	228	DQ50
103	VSS	104	CB7, NC	229	DQ51	230	VSS
105	CB0, NC	106	VSS	231	VSS	232	DQ60
107	VSS	108	RESET_n	233	DQ61	234	VSS
109	CKE0	110	CKE1	235	VSS	236	DQ57
111	VDD	112	VDD	237	DQ56	238	VSS
113	BG1	114	ACT_n	239	VSS	240	DQS7_c
115	BG0	116	ALERT_n	241	DM7_n/DBI7_n	242	DQS7_t
117	VDD	118	VDD	243	VSS	244	VSS
119	A12	120	A11	245	DQ62	246	DQ63
121	A9	122	A7	247	VSS	248	VSS
123	VDD	124	VDD	249	DQ58	250	DQ59
125	A8	126	A5	251	VSS	252	VSS

127	A6	128	A4	253	SCL	254	SDA
129	VDD	130	VDD	255	VDDSP	256	SA0
				257	VPP	258	VTT
				259	VPP	260	SA1

(16GB, 2Gbx64 Module -Populated as 2 ranks of x8 DDR4 SDRAMs) - Part 1 of 2



(16GB, 2Gbx64 Module -Populated as 2 ranks of x8 DDR4 SDRAMs) - Part 2 of 2